

## FEATURES

- 95 dB dynamic range
- -85 dB THD+N
- Up to 200 kHz sampling frequency
- I<sup>2</sup>S or Left Justified audio data format, 16-24 bits
- VDDA and VDDD from 3V to 5.5V
- VDDP from 1.4V to 5.5V
- Auto speed mode detection in slave mode.
- Auto MCLK divide detection in master mode.

## APPLICATIONS

- Digital Video Recorder
- Audio Recorder
- Set Top Boxes
- LCD or Digital TVs
- Car Audio
- A/V Receiver

## GENERAL DESCRIPTION

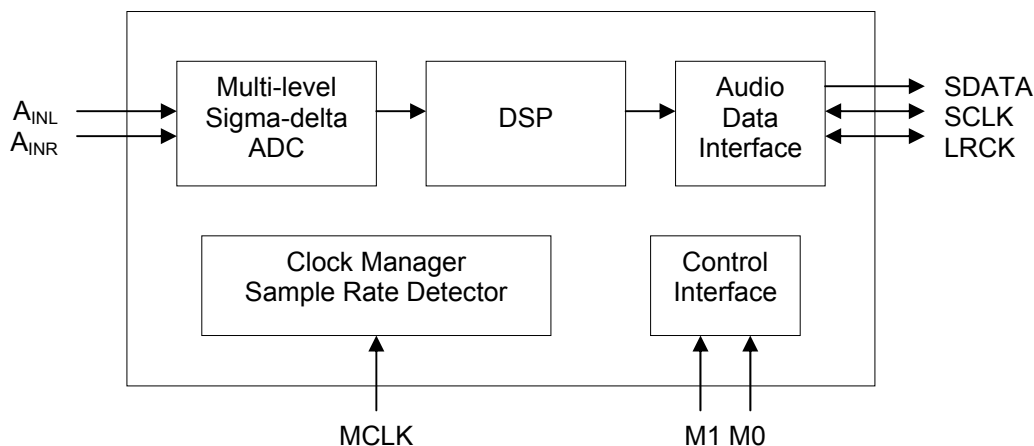
The PA5240 is a low cost stereo analog to digital converter.

The PA5240 can accept I<sup>2</sup>S or Left Justified serial audio data format up to 24-bit word length.

The device uses advanced multi-bit  $\Delta$ - $\Sigma$  modulation technique to convert signals from analog to digital.

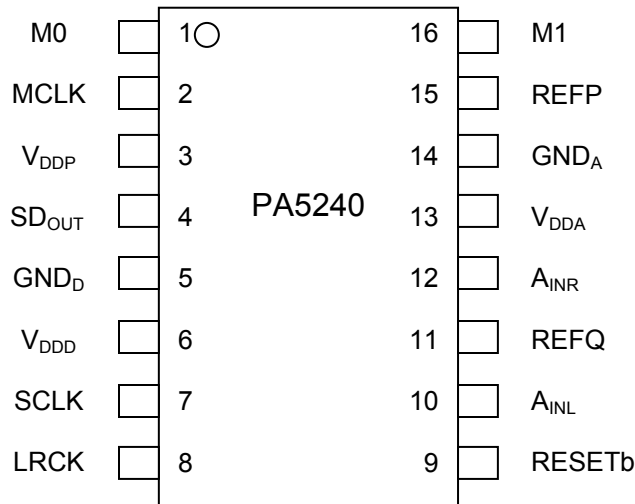
The multi-bit  $\Delta$ - $\Sigma$  modulator makes the device with very low sensitivity to clock jitter and very low out of band noise.

## BLOCK DIAGRAM



## ORDERING INFORMATION

Temperature Range	Package	Part Number
-40 to 85 °C	TSSOP-16	PA5240-T7

**PIN DESCRIPTIONS**


Pin Name	Pin number	Input or Output	Pin Description
M0, M1	1, 16	I	Mode selection
MCLK	2	I	Master clock
SCLK	7	I/O	Serial data bit clock
LRCK	8	I/O	Serial data left and right channel frame clock
SDOUT	4	O	Serial data output
RESETb	9	I	Active low chip reset
A <sub>INL</sub> , A <sub>INR</sub>	10,12	I	Analog left and right inputs
V <sub>DDP</sub>	3	I	Power supply for the digital input and output
V <sub>DD</sub> /GND <sub>D</sub>	6, 5	I	Digital power supply
V <sub>DDA</sub> /GND <sub>A</sub>	13, 14	I	Analog power supply
REFP	15	O	Filtering capacitor connection
REFQ	11	O	Filtering capacitor connection

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage ..... MIN -0.3V MAX +7.0V  
 Input Voltage ..... MIN GND-0.3V MAX V<sub>DDP</sub>+0.3V  
 Operating Temperature.....MIN -40°C MAX +85°C  
 Storage Temperature.....MIN -65°C MAX +150°C

**RECOMMENDED OPERATING CONDITIONS**

V<sub>DDA</sub> ..... MIN 3.0V MAX 5.5V  
 V<sub>DD</sub> ..... MIN 3.0V MAX 5.5V  
 V<sub>DDP</sub>..... MIN 1.5V MAX 5.5V

**ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS**

Test conditions are as the following unless otherwise specify:

$V_{DDA}=5V$ ,  $V_{DDD}=3.3V$ ,  $GND_A=0V$ ,  $GND_D=0V$ , Ambient temperature=25°C,  $F_s=48\text{ KHz}$ ,  $96\text{ KHz}$  or  $192\text{ KHz}$ ,  $MCLK/LRCK=256$  or  $128$

PARAMETER	MIN	TYP	MAX	UNIT
Dynamic Range (Note 1)		98		dB
THD+N		-85		dB
Channel Separation (1KHz)		85		dB
Signal to Noise ratio		98		dB
Interchannel Gain Mismatch		0.1		dB
Gain Error			5	%
<i>Filter Frequency Response – Single Speed</i>				
Passband	0		0.4535	Fs
Stopband	0.5465			Fs
Passband Ripple			±0.05	dB
Stopband Attenuation	70			dB
<i>Filter Frequency Response – Double Speed</i>				
Passband	0		0.4167	Fs
Stopband	0.5833			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
<i>Filter Frequency Response – Quad Speed</i>				
Passband	0		0.2083	Fs
Stopband	0.7917			Fs
Passband Ripple			±0.005	dB
Stopband Attenuation	70			dB
<i>Analog Input</i>				
Full Scale Input Level		1		Vrms
Input Impedance		20		KΩ

Note

1. The value is measured used A-weighted filter. If not use, the result will decrease 2-3 dB.

**SERIAL AUDIO PORT SWITCHING CHARACTERISTICS**

PARAMETER	SYMBOL	MIN	MAX	UNIT
MCLK Frequency			51.2	MHz
MCLK Duty Cycle		40	60	%
LRCK Frequency			200	KHz
LRCK Duty Cycle		40	60	%
SCLK Frequency			26	MHz
SCLK Pulse Width Low	$T_{SCKL}$	15		ns
SCLK Pulse Width High	$T_{SCKH}$	15		ns
SCLK Rising to LRCK Edge Delay	$T_{LRH}$	10		ns
SCLK Rising to LRCK Edge Setup Time	$T_{RSU}$	10		ns
SDATA Valid to SCLK Rising Setup Time	$T_{SDS}$	10		ns
SCLK Rising to SDATA Hold Time	$T_{SDH}$	10		ns

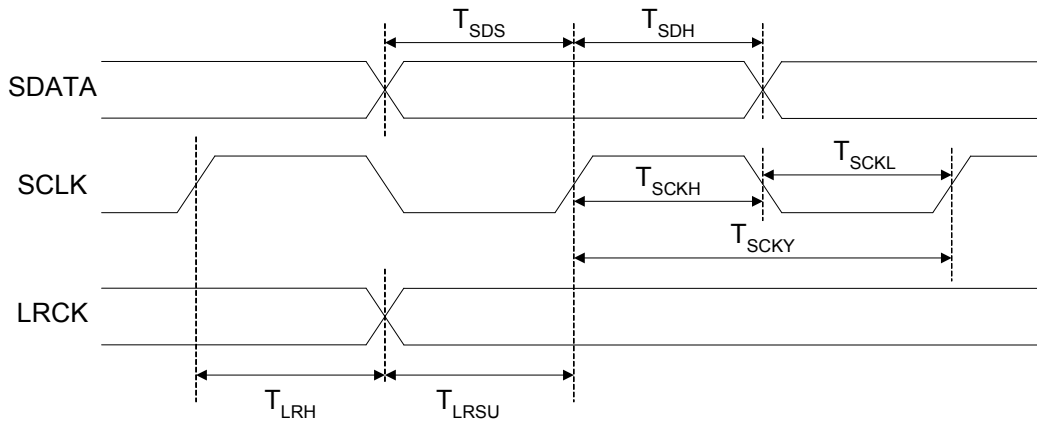


Figure 1 Serial Audio Port Timing



**DC CHARACTERISTICS AND SPECIFICATIONS**

PARAMETER	MIN	TYP	MAX	UNIT
Power Supply Current (Normal Operation Mode)				
$V_{DDA}=5V$ $V_{DDA}=3.3V$ $V_{DDD}, V_{DDP}=5V$ $V_{DDD}, V_{DDP}=3.3V$	IA	23.3		mA
	IA	21.1		mA
	ID	32		mA
	ID	14		mA
Power Supply Current (Power Down Operation Mode)				
$V_{DDA}=5V$ $V_{DDA}=3.3V$ $V_{DDD}, V_{DDP}=5V$ $V_{DDD}, V_{DDP}=3.3V$	IA	1.5		mA
	IA	1.2		mA
	ID	TBD		mA
	ID	1.1		mA
<b>Digital Voltage Level</b>				
Input High-level Voltage	$V_{IH}$	$0.7V_{DDP}$		V
Input Low-level Voltage	$V_{IL}$		$0.3V_{DDP}$	V
Output High-level Voltage	$V_{OH}$	$0.7V_{DDP}$		V
Output Low-level Voltage	$V_{OL}$		$0.1V_{DDP}$	V

**RECOMMENDED APPLICATION CIRCUIT**

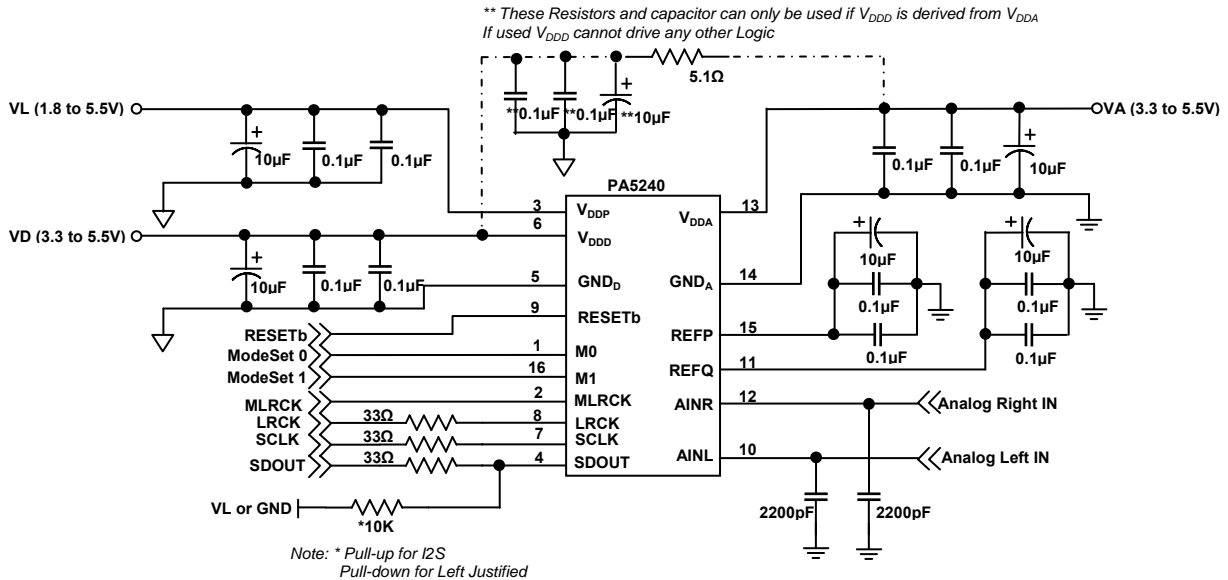


Figure 1 Recommended Application Circuit



## APPLICATION DESCRIPTIONS

### Master Clock Mode, Slave Clock Mode and Sampling Frequency

The device can work either in master clock mode or slave clock mode by setting mode control pins M1 and M0 according to Table 1.

**Table 1 Mode Control**

Pin	Input/Output	Pin Description
M1:M0	I	00 – master clock mode, single speed mode 01 – master clock mode, double speed mode 10 – master clock mode, quad speed mode 11 – slave clock mode, all speed modes

In master mode, LRCK and SCLK are derived internally from MCLK. The available MCLK/LRCK ratios are listed in Table 2. SCLK/LRCK ratio is always 64 in master mode.

In slave mode, LRCK and SCLK are supplied externally. LRCK and SCLK must be synchronously derived from the system clock with some specific rates. The device can auto detect MCLK/LRCK ratio according to Table 2. The device only supports the MCLK/LRCK ratios listed in Table 2. The LRCK/SCLK ratio is normally 64.

**Table 2. Sampling Frequency and MCLK/LRCK Ratio**

Speed Mode	MCLK/LRCK Ratio	Master Clock Mode Sampling Frequency	Slave Clock Mode Fs Auto Detection Range
Single Speed	512	43kHz – 50kHz	8kHz – 50kHz
	256	8kHz – 50kHz	
Double Speed	256	86kHz – 100kHz	84kHz – 100kHz
	128	50kHz – 100kHz	
Quad Speed	128	172kHz – 200kHz	167kHz – 200kHz
	64*	100kHz – 200kHz	

\*In Quad speed mode, 64 ratio only available in Master Mode

According to the sampling rate, the device can work in three speed modes: single speed, double speed and quad speed.

In master mode, mode pins M1 and M0 set the speed mode according to Table 1.

In slave mode, the device can detect the speed mode automatically when the sampling rate falls into the auto detection ranges listed in Table 2.

### Audio Data Output

PA5240 can accept I<sup>2</sup>S or Left Justified serial audio input data from 16-bit to 24-bit. The device can detect the data word length automatically. The relationship of SDATA, SCLK and LRCK with the two formats is shown through Figure 2 to Figure 3.

When device powers up, it will detect the logic level on SDOUT pin. If the logic level on SDOUT is high, PA5240 selects I<sup>2</sup>S format. If the logic level on SDOUT is low, PA5240 selects Left Justified format.

SDOUT pin can be pull-up by a 10kΩ resistor to set I<sup>2</sup>S audio format, or pull-down by a 10 kΩ resistor to set Left Justified format.

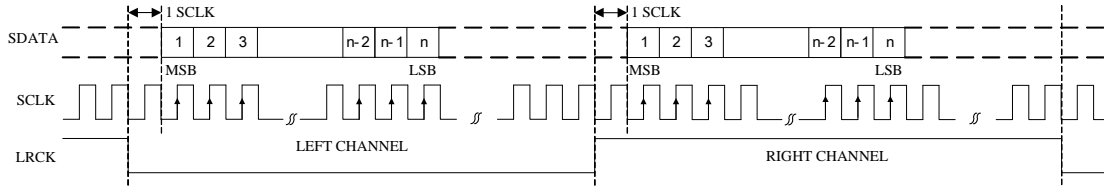


Figure 2 I²S Serial Audio Data Format Up To 24-bit

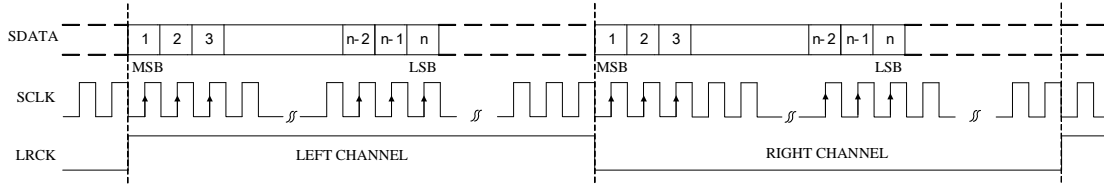


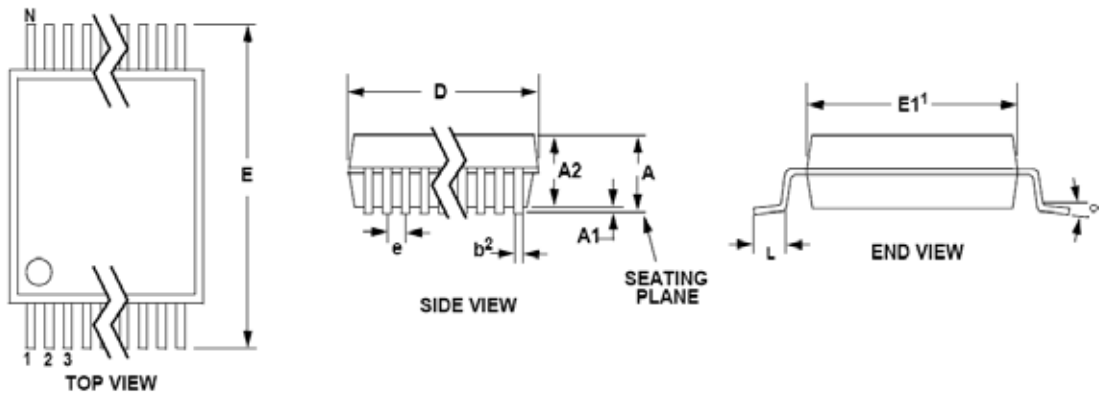
Figure 3 Left Justified Serial Audio Data Format Up To 24-bit

## POWER UP AND POWER DOWN

RESETb pin active low will put the device in power down mode. During power-up, RESETb pin should be hold at low level to keep the device in reset until the power supplies, clocks and mode selection pins are stable.

**PACKAGE INFORMATION**

**16L TSSOP (4.4 mm BODY) PACKAGE DRAWING**



DIM	INCHES			MILLIMETERS			NOTE
	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.193	0.1969	0.201	4.90	5.00	5.10	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	0.026 BSC	--	--	0.65 BSC	--	
L	0.020	0.024	0.028	0.50	0.60	0.70	
μ	0°	4°	8°	0°	4°	8°	

**Life Support Policy**

PROTEK ANALOG'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF PROTEK DEVICES.

