

## FEATURES

### ADC and DAC:

- 100 dB dynamic range
- -90 dB THD
- 8 kHz to 200 kHz sampling frequency
- I<sup>2</sup>S, left justified and right justified audio data format, 16-24 bits
- 128, 192, 256, 384, 512, 768 and 1024 MCLK to LRCK ratios
- Independent ADC and DAC sampling frequencies and clocks
- Advanced multi-bit delta-sigma with low sensitivity to clock jitter
- Single power supply from 3V to 5.5V
- Hardware mode or SPI or 2-wire uC interface

### ADC:

- 4-to-1 MUX for analog inputs
- Direct 2 V<sub>RMS</sub> analog input
- ADC PGA from 11.5 dB to -11.5 dB in 0.5 dB per step
- Digital attenuation from 6.5 dB to 89.5 dB in 0.5 dB per step
- Optional high pass filter to remove analog DC offset

### DAC:

- Digital volume control from 0 dB to 120 dB attenuation in 0.5 dB per step, with soft ramp and zero crossing transition
- De-emphasis filter for 32, 44.1 and 48 kHz sampling frequencies
- Selectable fast and slow roll-off filters
- 95 dB dynamic range
- -85 dB THD+N
- Up to 200 kHz sampling frequency
- I<sup>2</sup>S audio data format, 16-24 bits
- Single power supply 4.5 V to 5.5V

## APPLICATIONS

- DVD recorder
- Personal video recorder
- LCD and digital TVs
- Car audio
- AV receiver

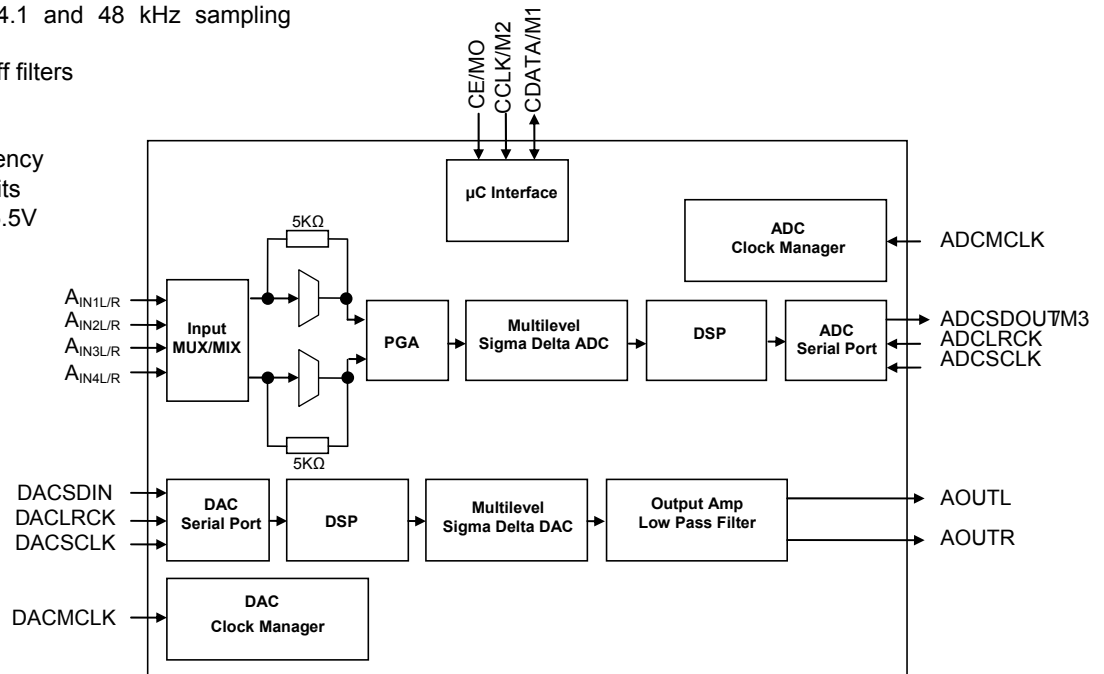
## GENERAL DESCRIPTION

PA5322 is a low cost high performance stereo audio CODEC. PA5322 performs stereo digital to analog conversion and analog to digital conversion continuously from 8 kHz to 200 kHz sampling frequency. PA5322 is ideal for high performance cost sensitive consumer audio applications.

PA5322 can accept I<sup>2</sup>S; left justified and right justified serial audio data formats up to 24-bit word length. ADC and DAC operate on independent sampling frequencies and clocks. The device uses advanced multi-bit ( $\Delta$ - $\Sigma$ ) delta-sigma modulation technique to convert data between digital and analog. The multi-bit ( $\Delta$ - $\Sigma$ ) delta-sigma modulators makes the device with low sensitivity to clock jitter and low out of band noise.

PA5322 can operate either in the hardware mod or the software mode. In the hardware mode, pin M0, M1, M2 and M3 set the operation of the device. In the software mode, PA5322 provides SPI or 2-wire micro-controller interfaces to configure its operations.

## BLOCK DIAGRAM



## ORDERING INFORMATION

| Temperature Range | Package | Part Number |
|-------------------|---------|-------------|
| -40 to 85 °C      | SSOP-28 | PA5322-T7   |

**PIN CONFIGURATION**

|             |    |    |         |
|-------------|----|----|---------|
| DACSDIN     | 1  | 28 | AOUTL   |
| DACLRCK     | 2  | 27 | AOUTR   |
| DACSCLK     | 3  | 26 | DACREFP |
| DACMCLK     | 4  | 25 | AIN4L   |
| ADCLRCK     | 5  | 24 | AIN3L   |
| ADCSCCLK    | 6  | 23 | AIN2L   |
| VDDD        | 7  | 22 | VDDA    |
| GNDD        | 8  | 21 | GNDA    |
| ADCMCLK     | 9  | 20 | AIN1L   |
| ADCSDOUT/M3 | 10 | 19 | AIN1R   |
| CCLK/M2     | 11 | 18 | AIN2R   |
| CDATA/M1    | 12 | 17 | AIN3R   |
| CE/M0       | 13 | 16 | AIN4R   |
| MUTE        | 14 | 15 | ADCREFP |

**PIN DESCRIPTIONS**

| Pin   | Pin No. | Pin Description  |
|---|---------|--|
| <i>ADC Pin.</i>                                   |         |  |
| A <sub>IN1L/R</sub>                               | 20, 19  | Analog input 1 left and right channels   |
| A <sub>IN2L/R</sub>                               | 23, 18  | Analog input 2 left and right channels   |
| A <sub>IN3L/R</sub>                               | 24, 17  | Analog input 3 left and right channels   |
| A <sub>IN4L/R</sub>                               | 25, 16  | Analog input 4 left and right channels   |
| ADC <sub>MCLK</sub>                               | 9       | ADC master clock   |
| ADC <sub>SDOUT/M3</sub>                           | 10      | ADC PCM serial data output   |
| AD <sub>CLRCK</sub>                               | 5       | ADC PCM serial data left and right channel frame clock   |
| ADC <sub>SCLK</sub>                               | 6       | ADC PCM serial data bit clock  |
| DAC <sub>MCLK</sub>                               | 4       | DAC master clock   |
| DAC <sub>SDIN</sub>                               | 1       | DAC PCM serial data input  |
| DA <sub>CLRCK</sub>                               | 2       | DAC PCM serial data left and right channel frame clock   |
| DAC <sub>SCLK</sub>                               | 3       | DAC PCM serial data bit clock  |
| A <sub>OUTL/R</sub>                               | 28, 27  | DAC analog output left and right channels  |
| MUTE  | 14      | Mute pin, active when detect 8K zero input in both left and right channels or users choose to mute the DAC |
| <i>DAC Pin.</i>                                   |         |  |
| CE/M0   | 13      | SPI uC interface chip select or 2-wire AD0   |
| CCLK/M2   | 11      | SPI or 2-wire (I2C compatible) uC interface clock  |
| CDATA/M1  | 12      | SPI or 2-wire (I2C compatible) uC interface data   |
| <i>Micro-Controller Pin or Hardware Mode Pin.</i> |         |  |
| V <sub>DDD</sub> /GND <sub>D</sub>                | 7, 8    | Digital power supply   |
| V <sub>DDA</sub> /GND <sub>A</sub>                | 22, 21  | Analog power supply  |
| ADC <sub>REFP</sub> /DAC <sub>REFP</sub>          | 15, 26  | Analog filtering pins  |

In hardware mode, the mode pins function as follows:

| Pin   | Pin No. | Pin Description  |
|-------|---------|--|
| M3    | 10      | External pull-up (47k resistor) – ADC and DAC I <sup>2</sup> S serial data format<br>External pull-down (47k resistor) – ADC and DAC LJ serial data format |
| M2    | 11      | 0 – no de-emphasis<br>1 – 44.1 kHz de-emphasis filter on   |
| M1:M0 | 12, 13  | 00 – select AIN1<br>01 – select AIN2<br>10 – select AIN3<br>11 – select AIN4   |

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... MIN-0.3V MAX +7.0V  
 Input Voltage ..... MIN GND-0.3V MAX V<sub>DD</sub>+0.3V  
 Operating Temperature.....MIN -40°C MAX +85°C  
 Storage Temperature.....MIN -65°C MAX +150°C

*Note: Continuous operation at or beyond these conditions may permanently damage the device.*

### RECOMMENDED OPERATING CONDITIONS

Analog Supply Voltage ..... MIN 3.0V MAX 5.5V  
 Digital Supply Voltage ..... MIN 3.0V MAX 5.5V

### ADC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS

Test conditions are as the following unless otherwise specify:

VDDA=+5.0V, VDDD=+5.0V, GNDA=0V, GNDD=0V, Ambient temperature=+25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

| PARAMETER                                       | MIN    | TYP | MAX    | UNIT |
|---|--------|-----|--------|------|
| <b>ADC Performance</b>                          |        |     |        |      |
| Dynamic Range (Note 1)                          | 85     | 95  | 100    | dB   |
| THD+N   | -90    | -86 | -80    | dB   |
| Channel Separation (1KHz)                       | 80     | 85  | 90     | dB   |
| Signal to Noise ratio                           | 85     | 95  | 100    | dB   |
| Inter-channel Gain Mismatch                     |        | 0.1 |        | dB   |
| Gain Error                                      |        |     | ±5     | %    |
| <b>Filter Frequency Response – Single Speed</b> |        |     |        |      |
| Pass-band                                       | 0      |     | 0.4535 | Fs   |
| Stop-band                                       | 0.5465 |     |        | Fs   |
| Pass-band Ripple                                |        |     | ±0.05  | dB   |
| Stop-band Attenuation                           | 70     |     |        | dB   |
| <b>Filter Frequency Response – Double Speed</b> |        |     |        |      |
| Pass-band                                       | 0      |     | 0.4167 | Fs   |
| Stop-band                                       | 0.5833 |     |        | Fs   |
| Pass-band Ripple                                |        |     | ±0.005 | dB   |
| Stop-band Attenuation                           | 70     |     |        | dB   |
| <b>Filter Frequency Response – Quad Speed</b>   |        |     |        |      |
| Pass-band                                       | 0      |     | 0.2083 | Fs   |
| Stop-band                                       | 0.7917 |     |        | Fs   |
| Pass-band Ripple                                |        |     | ±0.005 | dB   |

|                                 |    |            |  |                  |
|---------------------------------|----|------------|--|------------------|
| Stop-band Attenuation           | 70 |            |  | dB               |
| <b>Analog Input</b>             |    |            |  |                  |
| Full Scale Input Level (Note 2) |    | 2*(VDDA/5) |  | V <sub>rms</sub> |
| Input Impedance                 | 10 |            |  | KΩ               |

**Note**

1. The value is measured used A-weighted filter. If not use, the result will decrease 2-3 dB.
2. PA5322 allows direct 2 V<sub>RMS</sub> inputs if external 5 KΩ resistors are used in serial with the analog input pins. 1 V<sub>RMS</sub> inputs can directly apply to the analog input pins.

**DAC ANALOG AND FILTER CHARACTERISTICS AND SPECIFICATIONS**

Test conditions are as the following unless otherwise specify:

VDDA=+5.0V, VDDD=+5.0V, GNDA=0V, GNDD=0V, Ambient temperature=+25°C, Fs=48 KHz, 96 KHz or 192 KHz, MCLK/LRCK=256.

| PARAMETER   | MIN    | TYP  | MAX    | UNIT |
|---|--------|------|--------|------|
| <b>DAC Performance</b>  |        |      |        |      |
| Dynamic Range (Note 1)  | 85     | 98   | 100    | dB   |
| THD+N   | -90    | -82  | -75    | dB   |
| Channel Separation (1KHz)   | 80     | 85   | 90     | dB   |
| Signal to Noise ratio   | 85     | 97   | 100    | dB   |
| Inter-channel Gain Mismatch   |        | 0.05 |        | dB   |
| <b>Filter Frequency Response – Single Speed, Fast Roll-off Filter</b> |        |      |        |      |
| Pass-band   | 0      |      | 0.4535 | Fs   |
| Stop-band   | 0.5465 |      |        | Fs   |
| Pass-band Ripple  |        |      | ±0.05  | dB   |
| Stop-band Attenuation   | 53     |      |        | dB   |
| <b>Filter Frequency Response – Double Speed, Fast Roll-off Filter</b> |        |      |        |      |
| Pass-band   | 0      |      | 0.4167 | Fs   |
| Stop-band   | 0.5833 |      |        | Fs   |
| Pass-band Ripple  |        |      | ±0.005 | dB   |
| Stop-band Attenuation   | 56     |      |        | dB   |
| <b>Filter Frequency Response – Quad Speed, Fast Roll-off Filter</b>   |        |      |        |      |
| Pass-band   | 0      |      | 0.2083 | Fs   |
| Stop-band   | 0.7917 |      |        | Fs   |
| Pass-band Ripple  |        |      | ±0.006 | dB   |
| Stop-band Attenuation   | 50     |      |        | dB   |
| <b>Filter Frequency Response – Single Speed, Slow Roll-off Filter</b> |        |      |        |      |
| Pass-band   | 0      |      | 0.4167 | Fs   |
| Stop-band   | 0.5833 |      |        | Fs   |
| Pass-band Ripple  |        |      | ±0.05  | dB   |
| Stop-band Attenuation   | 65     |      |        | dB   |
| <b>Filter Frequency Response – Double Speed, Slow Roll-off Filter</b> |        |      |        |      |
| Pass-band   | 0      |      | 0.2083 | Fs   |
| Stop-band   | 0.7917 |      |        | Fs   |
| Pass-band Ripple  |        |      | ±0.005 | dB   |
| Stop-band Attenuation   | 85     |      |        | dB   |
| <b>Filter Frequency Response – Quad Speed, Slow Roll-off Filter</b>   |        |      |        |      |

|  |        |          |        |     |
|--|--------|----------|--------|-----|
| Pass-band  | 0      |          | 0.1042 | Fs  |
| Stop-band  | 0.8958 |          |        | Fs  |
| Pass-band Ripple   |        |          | ±0.005 | dB  |
| Stop-band Attenuation                                      | 55     |          |        | dB  |
| <b>De-emphasis Error at 1 KHz (Single Speed Mode Only)</b> |        |          |        |     |
| Fs = 32KHz   |        |          | 0.002  | dB  |
| Fs = 44.1KHz   |        |          | 0.013  |     |
| Fs = 48KHz   |        |          | 0.0009 |     |
| <b>Analog Output</b>                                       |        |          |        |     |
| Full Scale Output Level                                    |        | 0.7*VDDA |        | Vpp |
| Output Impedance   |        | 120      |        | Ω   |
| Load Resistance  | 2      |          |        | KΩ  |
| Load Capacitance   |        |          | 100    | PF  |

**Note**

1. The value is measured used A-weighted filter.

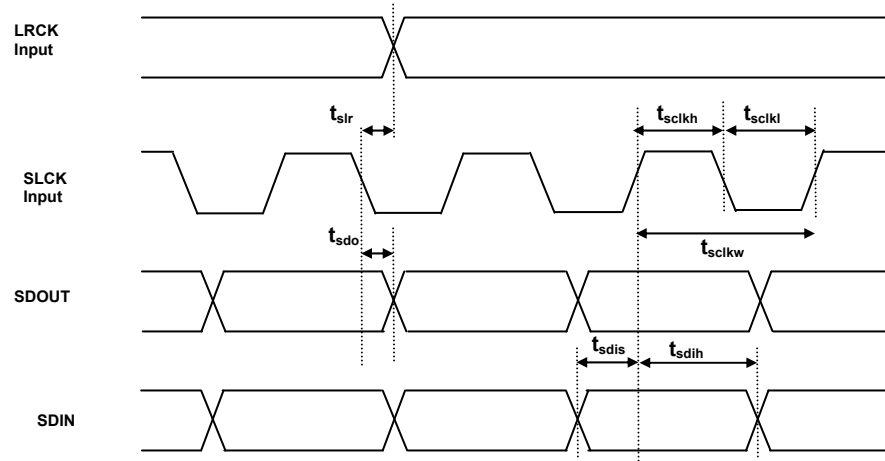
**DC CHARACTERISTICS AND SPECIFICATIONS**

| PARAMETER   | MIN | TYP              | MAX | UNIT |
|---|-----|------------------|-----|------|
| <b>Normal Operation Mode</b>  |     |                  |     |      |
| V <sub>DDD</sub> =V <sub>DDA</sub> =5.0V:<br>V <sub>DDD</sub> Current<br>V <sub>DDA</sub> Current |     | 42<br>55         |     | mA   |
| V <sub>DDD</sub> =V <sub>DDA</sub> =3.3V:<br>V <sub>DDD</sub> Current<br>V <sub>DDA</sub> Current |     | 34<br>50         |     |      |
| <b>Power Down Mode</b>  |     |                  |     |      |
| V <sub>DDD</sub> =V <sub>DDA</sub> =5.0V:<br>V <sub>DDD</sub> Current<br>V <sub>DDA</sub> Current |     | TBD<br>TBD       |     | mA   |
| V <sub>DDD</sub> =V <sub>DDA</sub> =3.3V:<br>V <sub>DDD</sub> Current<br>V <sub>DDA</sub> Current |     | TBD<br>TBD       |     |      |
| <b>Digital Voltage Level</b>  |     |                  |     |      |
| Input High-level Voltage  | 2.0 |                  |     | V    |
| Input Low-level Voltage   |     |                  | 0.8 | V    |
| Output High-level Voltage   |     | V <sub>DDD</sub> |     | V    |
| Output Low-level Voltage  |     | 0                |     | V    |
| Mute Pin Drive Capability   |     |                  | 3.0 | mA   |

**SERIAL AUDIO PORT SWITCHING SPECIFICATIONS**

| PARAMETER             | Symbol             | MIN | MAX  | UNIT |
|-----------------------|--------------------|-----|------|------|
| MCLK frequency        |                    |     | 51.2 | MHz  |
| MCLK duty cycle       |                    | 40  | 60   | %    |
| LRCK frequency        |                    |     | 200  | KHz  |
| LRCK duty cycle       |                    | 40  | 60   | %    |
| SCLK frequency        |                    |     | 26   | MHz  |
| SCLK pulse width low  | T <sub>SCLKL</sub> | 15  |      | ns   |
| SCLK Pulse width high | T <sub>SCLKH</sub> | 15  |      | ns   |

|                                      |            |     |    |    |
|--------------------------------------|------------|-----|----|----|
| SCLK falling to LRCK edge            | $T_{SLR}$  | -10 | 10 | ns |
| SCLK falling to SDOUT valid          | $T_{SDO}$  | 0   |    | ns |
| SDIN valid to SCLK rising setup time | $T_{SDIS}$ | 10  |    | ns |
| SCLK rising to SDIN hold time        | $T_{SDIH}$ | 10  |    | ns |

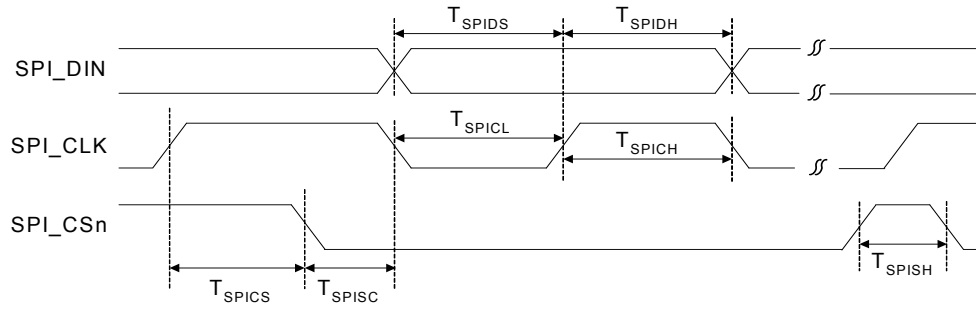


Serial Audio Port Timing

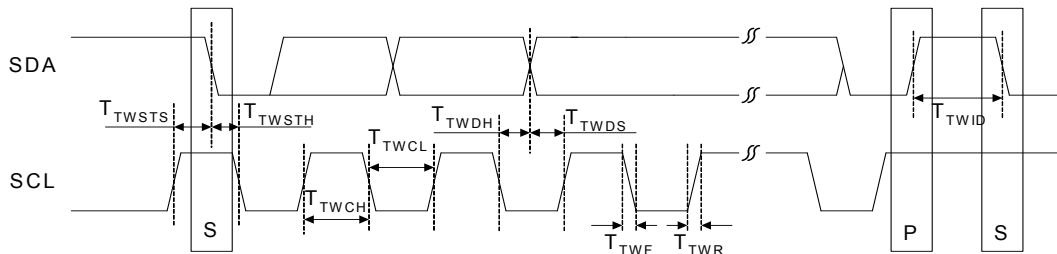
### SERIAL CONTROL PORT SWITCHING SPECIFICATIONS

| PARAMETER   | Symbol      | MIN | MAX | UNIT |
|---|-------------|-----|-----|------|
| <b>SPI Mode</b>                                     |             |     |     |      |
| SPI_CLK clock frequency                             |             |     | 10  | MHz  |
| SPI_CLK edge to SPI_CS <sub>n</sub> falling         | $T_{SPICS}$ | 5   |     | ns   |
| SPI_CS <sub>n</sub> High Time Between transmissions | $T_{SPISH}$ | 500 |     | ns   |
| SPI_CS <sub>n</sub> falling to SPI_CLK edge         | $T_{SPISC}$ | 10  |     | ns   |
| SPI_CLK low time                                    | $T_{SPICL}$ | 45  |     | ns   |
| SPI_CLK high time                                   | $T_{SPICH}$ | 45  |     | ns   |
| SPI_DIN to SPI_CLK rising setup time                | $T_{SPIDS}$ | 10  |     | ns   |
| SPI_CLK rising to DATA hold time                    | $T_{SPIDH}$ | 15  |     | ns   |
| <b>2-wire Mode</b>                                  |             |     |     |      |
| SCL Clock Frequency                                 | $F_{SCL}$   |     | 100 | KHz  |
| Bus Free Time Between Transmissions                 | $T_{TWID}$  | 4.7 |     | us   |
| Start Condition Hold Time                           | $T_{TWSTH}$ | 4.0 |     | us   |
| Clock Low time                                      | $T_{TWCL}$  | 4.0 |     | us   |
| Clock High Time                                     | $T_{TWCH}$  | 4.0 |     | us   |
| Setup Time for Repeated Start Condition             | $T_{TWSTS}$ | 4.7 |     | us   |
| SDA Hold Time from SCL Falling                      | $T_{TWDH}$  | 0.1 |     | us   |
| SDA Setup time to SCL Rising                        | $T_{TWDS}$  | 100 |     | ns   |
| Rise Time of SCL                                    | $T_{TWR}$   |     | 25  | us   |
| Fall Time SCL                                       | $T_{TWF}$   |     | 25  | ns   |



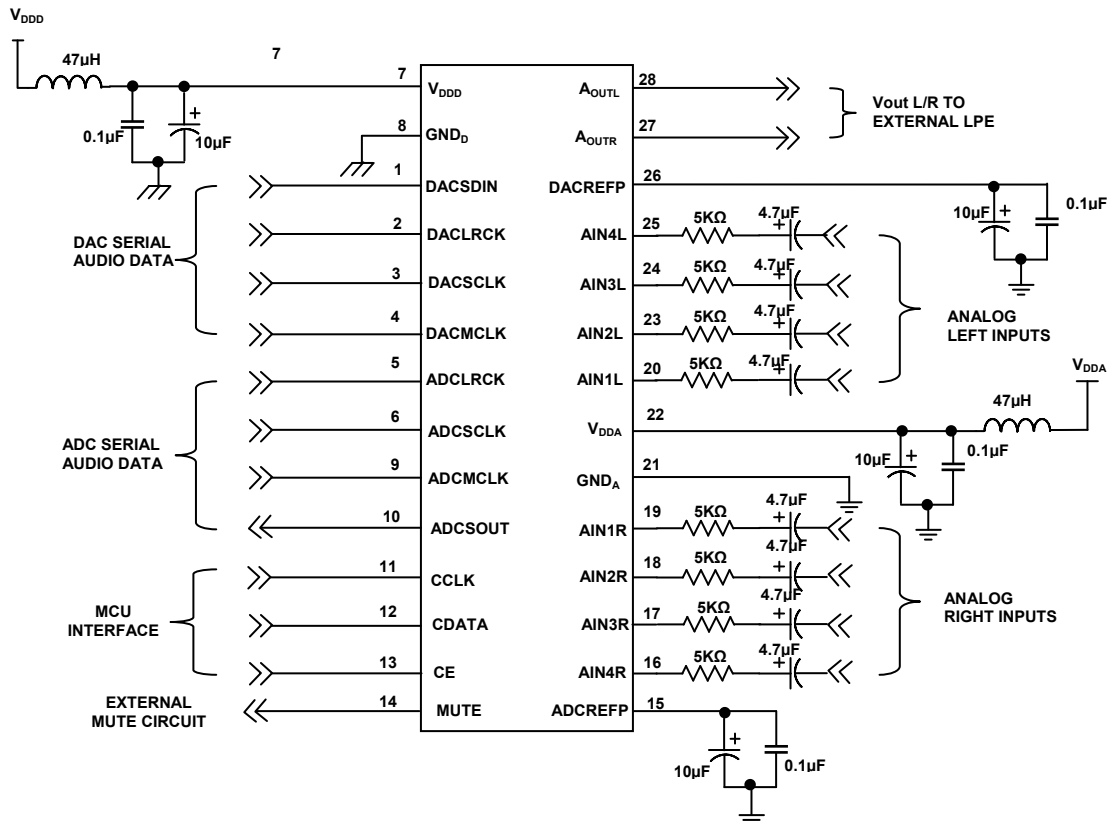


Serial Control Port SPI Timing



Serial Control Port 2-wire Timing

**RECOMMENDED APPLICATION CIRCUIT**



### AUDIO DATA SAMPLING FREQUENCY AND CLOCKS

According to the input serial audio data sampling frequency, the device can work in three speed modes: single speed, double speed or quad speed modes. The ranges of the sampling frequency in these three modes are listed in Table1.

ADCSampleRate bits in ADC Control 2 register (RAM address 0x02) or DACSampleRate bits in DAC Control 2 register (RAM address 0x07) set the speed mode.

By default, the device can detect the speed mode automatically when sampling rate falls within the Fs Auto Detection Ranges listed in Table1.

In this auto detection mode, sampling frequency outside the specified ranges is not supported. ADC and DAC have separate auto detection so ADC and DAC sampling frequencies can be completely independent.

Table 1. Sampling Frequency and CLK/LRCK Ration

| Speed Mode   | Sampling Frequency | Fs Auto Detection Range | MCLK/LRCK Ratio          |
|--------------|--------------------|-------------------------|--------------------------|
| Single Speed | 8kHz – 50kHz       | 8kHz – 50kHz            | 256, 384, 512, 768, 1024 |
| Double Speed | 50kHz – 100kHz     | 84kHz – 100kHz          | 128, 192, 256, 384, 512  |
| Quad Speed   | 100kHz – 200kHz    | 167kHz – 200kHz         | 128, 192, 256            |

The device uses separate master clocks, LRCK clocks and SCLK clocks for the ADC and DAC. The allowed MCLK/LRCK ratios in each speed mode are also listed in Table1. The device always detects MCLK/LRCK ratio automatically.

### HARDWARE MODE

The device can operate in the hardware mode or the software mode. The default is the hardware mode. To change the hardware mode to the software mode, set SCPEn bit of Chip Control register (RAM address 0x00) to 1.

In the hardware mode, pin M3 sets I<sup>2</sup>S or left justified ADC and DAC serial port mode, pin M2 sets DAC de-emphasis filter on or off, and pins M1 and pin M0 select one of the four ADC analog inputs.

Please refer to PIN DESCRIPTIONS section for detail settings.

### POWER UP AND DOWN

The chip internal power on reset will reset the device when VDDD ramps from ground to supply voltage level. When VDDD and VDDA are present to the device, applying ADCMCLK and ADCLRCK will startup the ADC and applying DACMCLK and DACLRCK will start up the DAC.

During the DAC startup, DAC analog outputs ramp gradually from ground to mid level to minimize audible pop noise. This gradual ramp feature can be turned off by setting ClickFree bit of DAC Control 1 register (RAM address 0x06) to 0.

ADC and DAC can power up or down independently. In the software mode, ADC or DAC can power down through ADCPDN bit or DACPDN bit of Chip Control register (RAM address 0x00). In the hardware mode, ADC can power down by stopping ADCMCLK or ADCLRCK, and DAC can power down by stopping DACMCLK or DACLRCK.

### MICRO-CONTROLLER CONFIGURATION INTERFACE

The device supports standard SPI and 2-wire micro-controller configuration interface. External micro-controller can completely configure the device through writing to internal configuration registers.

The identical device pins are used to configure either SPI or 2-wire interface. In SPI mode, pin CE, CCLK and CDATA function as SPI\_CSn, SPI\_CLK and SPI\_DIN. In 2-wire mode, pin CE, CCLK and CDATA function as AD0, SCL and SDA.

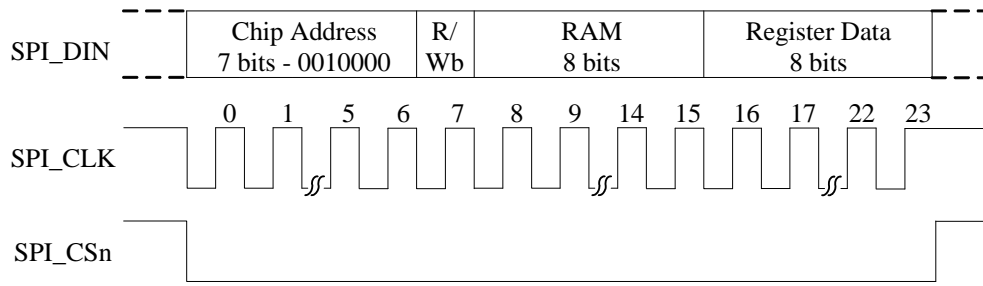
To select SPI mode, apply high to low transition signal to CE pin. Otherwise the device will operate in 2-wire interface mode.

### SPI

PA5322 has a SPI (Serial Peripheral Interface) compliant synchronous serial slave controller inside the chip. It provides the ability to allow the external master SPI controller to access the internal registers, and thus control the operations of chip.

All lines on the SPI bus are unidirectional: The SPI\_CLK is generated by the master controller and is primarily used to synchronize data transfer, the SPI\_DIN line carries data from the master to the slave; SPI\_CSn is generated by the master to select PA5322.

The timing diagram of this interface is given in Figure 1. The high to low transition at SPI\_CSn pin indicates the SPI interface selected. Each write procedure contains 3 words, i.e. Chip Address plus R/W bit, internal register address and internal register data. Every word length is fixed at 8 bits. The input SPI\_DIN data are sampled at the rising edge of SPI\_CLK clock. The MSB bit in each word is transferred firstly. The transfer rate can be up to 10M bps.



RAM = Register Address Mapping  
Figure1. SPI Configuration Interface Timing Diagram

**2-WIRE**

2-wire interface is a bi-directional serial bus that uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. The timing diagram for data transfer of this interface is given in Figure 2. Data are transmitted synchronously to SCL clock on the SDA line on a byte-by-byte basis. Each bit in a byte is sampled during SCL high with MSB bit being transmitted firstly. Each transferred byte is followed by an acknowledge bit from receiver to pull the SDA low. The transfer rate of this interface can be up to 100k bps.

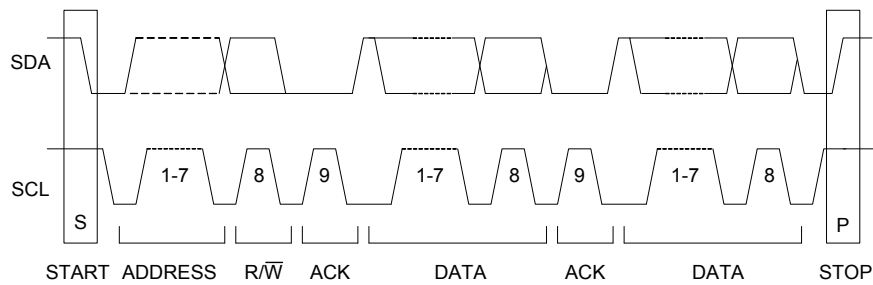


Figure2. Complete Data Transfer 2-wire Interface

A master controller initiates the transmission by sending a “start” signal, which is defined as a high-to-low transition at SDA while SCL is high. The first byte transferred is the slave address. It is a seven-bit chip address followed by a RW bit. The chip address must be 001000x, where x equals AD0 (pin CE). The RW bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the RW bit. The master can terminate the communication by generating a “stop” signal, which is defined as a low-to-high transition at SDA while SCL is high.

In 2-wire interface mode, the registers can be written and read. The formats of “write” and “read” instructions are shown in Table 2 and Table 3. Please note that, to read data from a register, you must set R/W bit to 0 to access the register address and then set R/W to 1 to read data from the register. There are no acknowledge bit after data to be written or read, this is the only difference from the I<sup>2</sup>C protocol.

Table 2 Write Data to Register in 2-wire Interface Mode

| Chip Address | R/W | Register Address | Data to be written              |
|--------------|-----|------------------|---------------------------------|
| 001000       | AD0 | 0                | ACK      RAM      ACK      DATA |

Table 3 Read Data from Register in 2-wire Interface Mode

| Chip Address | R/W | Register Address | Data to be read |
|--------------|-----|------------------|-----------------|
| 001000       | AD0 | 0                | ACK      RAM    |
| 001000       | AD0 | 1                | ACK      DATA   |



**CONFIGURATION REGISTER DEFINITION**

SPI and 2-wire configuration interface share the same registers because there is only one interface active at any time. There are total of 11 user programmable 8-bit registers in this device.

These registers control the operations of ADC and DAC. External master controller can access these registers by using the slave address specified in RAM (Register Address Map) register as shown in Table 2.

Table 2 Bit Content of Register Address Map

| Bit Name    | Bit | Description  |
|-------------|-----|--|
| RAM Address | 7:0 | The address of the register to be accessed:<br>0x00 – Chip Control (default)<br>0x01 – ADC Control 1<br>0x02 – ADC Control 2<br>0x03 – ADC Mute Control<br>0x04 – ADC Left Gain Control<br>0x05 – ADC Right Gain Control<br>0x06 – DAC Control 1<br>0x07 – DAC Control 2<br>0x08 – DAC Mute Control<br>0x09 – DAC Left Volume Control<br>0x0a – DAC Right Volume Control |

**Chip Control – 0x00**

| Bit Name | Bit | Description   |
|----------|-----|---|
| SCPEn    | 7   | 0 – hardware mode (default)<br>1 – software (control port) mode |
| Reserved | 6:5 | Reserved  |
| ADCPDN   | 4   | 0 – normal (default)<br>1 – ADC low power mode                  |
| Reserved | 3   | Reserved  |
| DACPDN   | 2   | 0 – normal (default)<br>1 – DAC low power mode                  |
| Reserved | 1:0 | Reserved  |

**ADC Control 1 – 0x01**

| Bit Name | Bit | Description   |
|----------|-----|---|
| AINMIX   | 7:3 | 00000 – AIN1 input to ADC (default)<br>xxxx1 – AIN1 input ADC<br>xxx1x – AIN2 input ADC<br>xx1xx – AIN3 input ADC<br>x1xxx – AIN4 input ADC<br>1xxxx – AIN5 input ADC |
| HPF      | 2   | 0 – ADC HPF enable (default)<br>1 – ADC HPF disable   |
| Reserved | 1:0 | Reserved  |

**ADC Control 2 – 0x02**

| Bit Name      | Bit | Description   |
|---------------|-----|---|
| ADCSampleRate | 7:6 | 00 – ADC speed mode auto detect (default)<br>01 – single speed mode<br>10 – double speed mode<br>11 – quad speed mode |

|               |     |  |
|---------------|-----|--|
| ADCSPDataMode | 5:3 | 000 – Left justified, up to 24 bit data<br>001 – I <sup>2</sup> S, up to 24 bit data (default)<br>010 – Right justified, 16 bit data<br>011 – Reserved<br>100 – Reserved<br>101 – Right justified, 24 bit data<br>110 – Reserved<br>111 – Reserved |
| SCLKRatio     | 2:1 | 00 – 32<br>01 – 48<br>10 – 64 (default)<br>11 – 128  |
| Reserved      | 0   | Reserved   |

**ADC Mute Control – 0x03**

| Bit Name    | Bit | Description   |
|-------------|-----|---|
| ADCMute     | 7   | 0 – normal (default)<br>1 – mute ADC digital output   |
| Reserved    | 6   | Reserved  |
| ADCRampRate | 5:4 | These bits define ADC gain control ramp rate:<br>00 – 0.5 dB per 4 LRCK (default)<br>01 – 0.5 dB per 8 LRCK<br>10 – 0.5 dB per 16 LRCK<br>11 – 0.5 dB per 32 LRCK |
| ADCL=R      | 3   | 0 – normal (default)<br>1 – both channel gain control is set by ADC Left Gain Control register  |
| ADCSoftRamp | 2   | ADC soft ramp at mute or gain change:<br>0 – Disabled<br>1 – Enabled (default)  |
| ADCZeroCrS  | 1   | ADC mute or gain change at zero crossing signal level to minimize audible noise<br>0 – Disabled<br>1 – Enabled (default)  |
| Reserved    | 0   | Reserved  |

**ADC Left Gain Control – 0x04**

| Bit Name | Bit | Description  |
|----------|-----|--|
| ADCGainL | 7:0 | 1110 1000 – 6.0 dB gain (PGA)<br>1110 1001 – 6.5 dB gain (PGA)<br>1110 1010 – 7.0 dB gain (PGA)<br>1110 1011 – 7.5 dB gain (PGA)<br>1110 1100 – 8.0 dB gain (PGA)<br>1110 1101 – 8.5 dB gain (PGA)<br>1110 1110 – 9.0 dB gain (PGA)<br>1110 1111 – 9.5 dB gain (PGA)<br>1111 0000 – 10.0 dB gain (PGA)<br>1111 0001 – 10.5 dB gain (PGA)<br>1111 0010 – 11.0 dB gain (PGA)<br>1111 0011 – 11.5 dB gain (PGA)<br>1111 0100 – 6.0 dB attenuation (PGA)<br>1111 0101 – 5.5 dB attenuation (PGA)<br>1111 0110 – 5.0 dB attenuation (PGA)<br>1111 0111 – 4.5 dB attenuation (PGA)<br>1111 1000 – 4.0 dB attenuation (PGA)<br>1111 1001 – 3.5 dB attenuation (PGA) |

|  |  |  |
|--|--|--|
|  |  | 1111 1010 – 3.0 dB attenuation (PGA)<br>1111 1011 – 2.5 dB attenuation (PGA)<br>1111 1100 – 2.0 dB attenuation (PGA)<br>1111 1101 – 1.5 dB attenuation (PGA)<br>1111 1110 – 1.0 dB attenuation (PGA)<br>1111 1111 – 0.5 dB attenuation (PGA)<br><b>0000 0000 – no gain or attenuation (default)</b><br>0000 0001 – 0.5 dB gain (PGA)<br>0000 0010 – 1.0 dB gain (PGA)<br>0000 0011 – 1.5 dB gain (PGA)<br>0000 0100 – 2.0 dB gain (PGA)<br>0000 0101 – 2.5 dB gain (PGA)<br>0000 0110 – 3.0 dB gain (PGA)<br>0000 0111 – 3.5 dB gain (PGA)<br>0000 1000 – 4.0 dB gain (PGA)<br>0000 1001 – 4.5 dB gain (PGA)<br>0000 1010 – 5.0 dB gain (PGA)<br>0000 1011 – 5.5 dB gain (PGA)<br>0000 1100 – 6.0 dB gain (PGA)<br>0000 1101 – 11.5 dB attenuation (PGA)<br>0000 1110 – 11.0 dB attenuation (PGA)<br>0000 1111 – 10.5 dB attenuation (PGA)<br>0001 0000 – 10.0 dB attenuation (PGA)<br>0001 0001 – 9.5 dB attenuation (PGA)<br>0001 0010 – 9.0 dB attenuation (PGA)<br>0001 0011 – 8.5 dB attenuation (PGA)<br>0001 0100 – 8.0 dB attenuation (PGA)<br>0001 0101 – 7.5 dB attenuation (PGA)<br>0001 0110 – 7.0 dB attenuation (PGA)<br>0001 0111 – 6.5 dB attenuation (PGA)<br>0001 1000 – 6.0 dB attenuation (PGA)<br>0001 1001 – 6.5 dB attenuation (6 dB PGA + digital attenuation)<br>0001 1010 – 7.0 dB attenuation (6 dB PGA + digital attenuation)<br>.....<br>1011 1111 – 89.5 dB attenuation (6 dB PGA + digital attenuation) |
|--|--|--|

**ADC Right Gain Control – 0x05**

| Bit Name | Bit | Description                                     |
|----------|-----|---|
| ADCGainR | 7:0 | Same as ADCGainL settings for ADC right channel |

**DAC Control 1 – 0x06**

| Bit Name     | Bit | Description   |
|--------------|-----|---|
| Reserved     | 7:6 | Reserved  |
| ClickFree    | 5   | 0 – disable pop noise suppression power up and down<br>1 – enable pop noise suppression power up and down (default) |
| SlowFilter   | 4   | 0 – fast filter roll off (default)<br>1 – slow filter roll off  |
| InvL<br>InvR | 3:2 | 0 – DAC analog output no phase inversion (default)<br>1 – DAC analog output 180 degree phase inversion              |
| Reserved     | 1:0 | Reserved  |

**DAC Control 2 – 0x07**

| Bit Name      | Bit | Description   |
|---------------|-----|---|
| DACSampleRate | 7:6 | 00 – DAC speed mode auto detect (default)<br>01 – single speed mode<br>10 – double speed mode<br>11 – quad speed mode |

|                |     |  |
|----------------|-----|--|
| DACSPDataMode  | 5:3 | 000 – Left justified, up to 24 bit data<br>001 – I <sup>2</sup> S, up to 24 bit data (default)<br>010 – Right justified, 16 bit data<br>011 – Reserved<br>100 – Reserved<br>101 – Right justified, 24 bit data<br>110 – Reserved<br>111 – Reserved |
| DeEmphasisMode | 2:1 | 00 – De-emphasis filter disabled (default)<br>01 – De-emphasis filter for Fs=32 KHz<br>10 – De-emphasis filter for Fs=44.1 KHz<br>11 – De-emphasis filter for Fs=48 KHz  |
| Reserved       | 0   | Reserved   |

**DAC Mute Control – 0x08**

| Bit Name    | Bit | Description  |
|-------------|-----|--|
| DACMute     | 7   | 0 – un-mute analog outputs for both channels (default)<br>1 – mute analog outputs for both channels  |
| DACRampRate | 6   | These bits define volume control ramp rate:<br>00 – 0.5 dB per 4 LRCK (default)<br>01 – 0.5 dB per 8 LRCK<br>10 – 0.5 dB per 16 LRCK<br>11 – 0.5 dB per 32 LRCK            |
| AutoMute    | 5   | Auto mute function: long period of zero inputs (8k audio samples) will mute the analog output. Any single non-zero input will un-mute. 0 – disable<br>1 – enable (default) |
| DACL=R      | 4   | 0 – normal (default)<br>1 – both channel volume control is set by Left Volume Control register   |
| DACSoftRamp | 3   | Soft ramp at mute and volume change:<br>0 – Disabled<br>1 – Enabled (default)  |
| DACZeroCrS  | 1   | Mute or volume change at zero crossing signal level to minimize audible noise<br>0 – Disabled<br>1 – Enabled (default)   |
| Reserved    | 0   | Reserved   |

**DAC Left Volume Control – 0x09**

| Bit Name   | Bit | Description  |
|------------|-----|--|
| DACVolumeL | 7:0 | Digital volume control setting attenuates the signal in 0.5 dB incremental from 0 to –120 dB. Max setting is –120 dB.<br>0000 0000 – no attenuation (default)<br>0000 0001 – 0.5 dB attenuation<br>0000 0010 – 1.0 dB attenuation<br>0000 0011 – 1.5 dB attenuation<br>..... |

**DAC Right Volume Control – 0x0a**

| Bit Name   | Bit | Description                                       |
|------------|-----|---|
| DACVolumeR | 7:0 | Same as DACVolumeL settings for DAC right channel |

**Digital Audio Interface**

The device provides three formats of serial audio data interface to the input of the DAC or output from the ADC through LRCK, SCLK and SDIN/SDOUT pins. The three formats are I<sup>2</sup>S, left justified and right justified. In the hardware mode, the formats are selected through pin M3.

In the software mode, the formats are selected by ADCSPDataMode bits of ADC Control 2 register (RAM address 0x02) or DACSPDataMode bits DAC Control 2 register (RAM address 0x07). DACSDIN is sampled by PA5322 on the rising edge of DACSCLK. ADC data is out on ADCSDOUT and changes on the falling edge of ADCSCLK. The relationship of SDATA (SDIN/SDOUT), SCLK and LRCK with the three formats is shown below through Figure 3 to Figure 5.

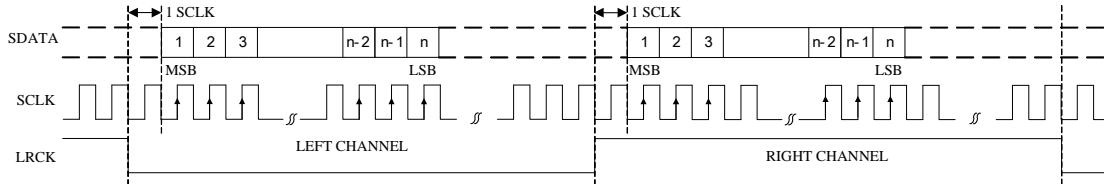


Figure 3. I<sup>2</sup>S Audio Data Format up to 24-bit

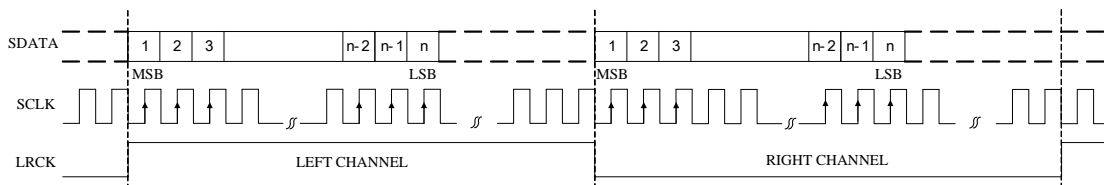


Figure 4. Left Justified Audio Data Format up to 24-bit

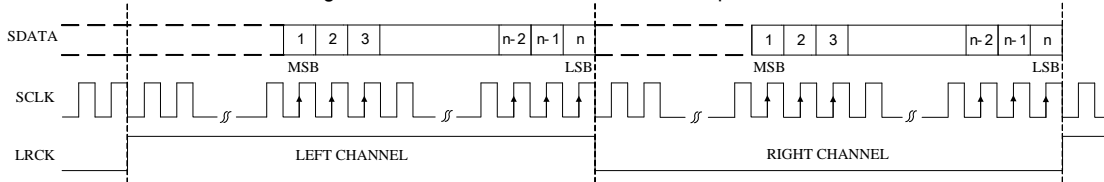


Figure 5. Right Justified Audio Data Format up to 24-bit

### Analog Input Multiplex and Programmable Gain Control

PA5322 allows direct 2  $V_{RMS}$  inputs if external 5 k $\Omega$  resistors are used in serial with the analog input pins. Please refer to Figure 6.  $V_{RMS}$  inputs can directly apply to the analog input pins.

In the hardware mode, the analog input is selected through mode pins M1 and M0. In the software mode, the analog input is selected through AINMIX bits of ADC Control 1 register (RAM address 0x01). In the software mode, more than one input can apply to the analog input pins to achieve mixing effects.

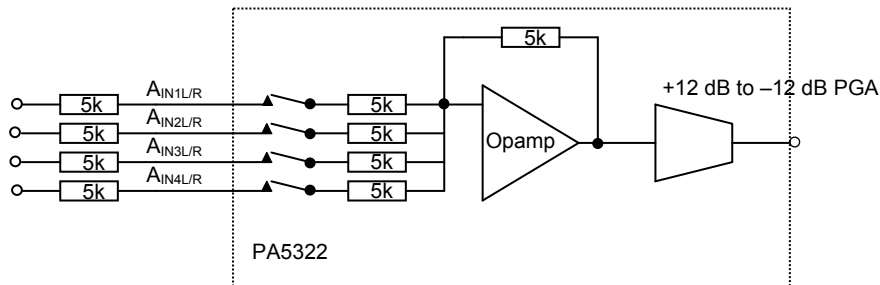


Figure 6. ADC Left and Right Inputs

The ADC has an analogue input PGA and digital gain control for each stereo channel. The analog PGA has a range of +12 dB to -12 dB gains in 0.5 dB per step. The digital gain control allows further attenuation (after the PGA) from 12.5 dB to 96 dB in 0.5 dB per step. ADC Left Gain Control register (RAM address 0x04) and ADC Right Gain Control register (RAM address 0x05) allows independent control of left and right channel gains.

Zero crossing detection and soft ramp control circuits are provided for the ADC gain control (ADC Mute Control register, RAM address 0x03). This feature minimizes the audible click and “zipper” noise as the gain values change.

#### DAC Fade In and Fade Out Transition

When DACMute bit in DAC Mute Control register (RAM address 0x08) is set, the analog outputs go to mute level (common mode voltage) gradually at the rate set by DACRampRate bits in the same register. Upon the release of the DACMute bit, the analog outputs go up gradually at the same rate set by DACRampRate bits. Please refer to Figure 7. The fade in and fade out feature can be set or disabled by DACSoftRamp bit in the same register.

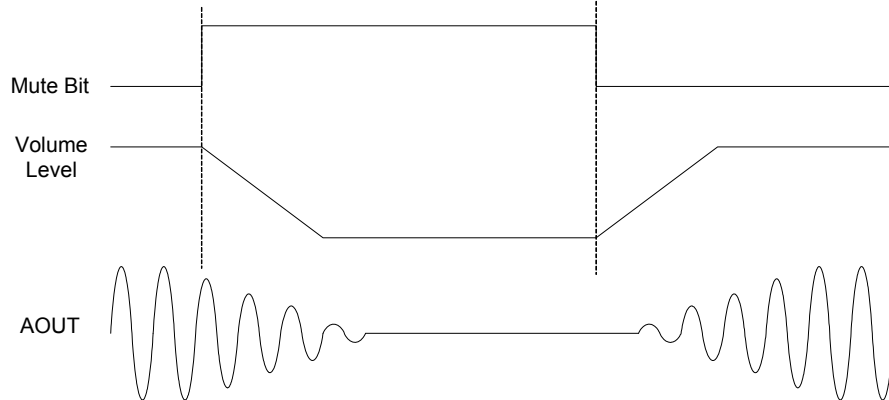
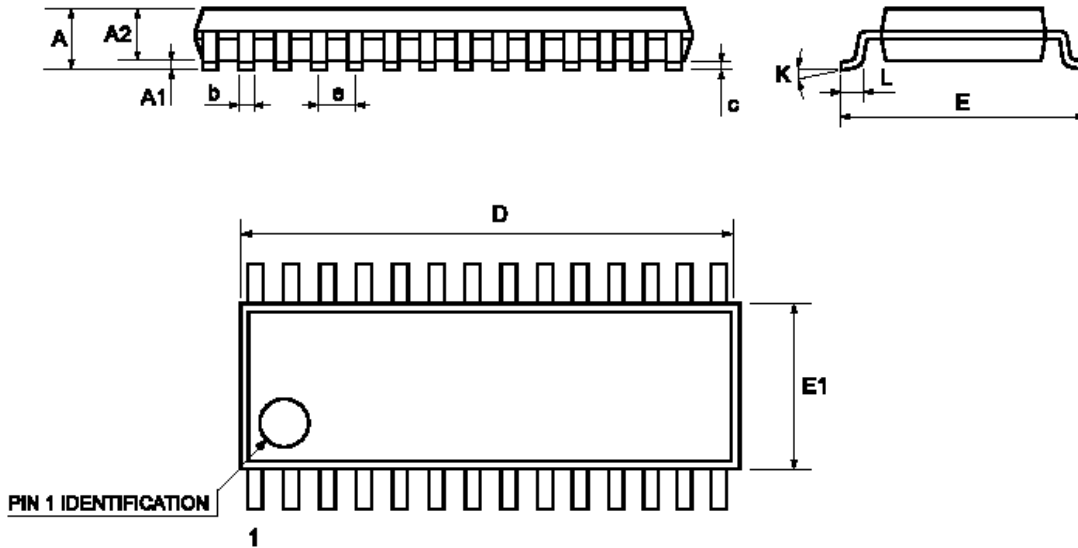


Figure 7. Fade In/Out Diagram

The fade in and fade out feature is also available when AutoMute bit in DAC Mute Control register (RAM address 0x08) is set to detect long stream of zero input data.

**PACKAGE DIMENSIONS AND MEASUREMENTS**

28-pin SSOP Outline Dimensions



| DIMENSIONS |       |      |      |       |        |       |
|------------|-------|------|------|-------|--------|-------|
| REF.       | mm    |      |      | inch  |        |       |
|            | MIN.  | TYP. | MAX. | MIN.  | TYP.   | MAX.  |
| A          |       |      | 2    |       |        | 0.079 |
| A1         | 0.050 |      |      | 0.002 |        |       |
| A2         | 1.65  | 1.75 | 1.85 | 0.065 | 0.069  | 0.073 |
| b          | 0.22  |      | 0.38 | 0.009 |        | 0.015 |
| c          | 0.09  |      | 0.25 | 0.004 |        | 0.010 |
| D          | 9.9   | 10.2 | 10.5 | 0.390 | 0.402  | 0.413 |
| E          | 7.4   | 7.8  | 8.2  | 0.291 | 0.307  | 0.323 |
| E1         | 5     | 5.3  | 5.6  | 0.197 | 0.209  | 0.220 |
| e          |       | 0.65 |      |       | 0.0256 |       |
| K          | 0°    |      | 10°  | 0°    |        | 10°   |
| L          | 0.55  | 0.75 | 0.95 | 0.022 | 0.030  | 0.037 |

**Life Support Policy**

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