

Features

Wide operating voltage range: 4.5 V to 13.2 V
 12 V_{PP} analog signal capability
 Internal latches and address decoder
 Full CMOS switch for low distortion
 Minimum feed-through and cross-talk
 Low power consumption
 R_{ON} < 65 Ω @ V_{DD} = 12 V, 25 °C.

Applications

PBX Systems
 Mobile radio
 Key systems
 Analog/Digital Multiplexers
 Audio/Video switching

Description

The Protek PMT8816 is a low power, highly reliable device. The device contains an 8 X 16 array of cross-point switches along with a 7 to 128 line decoder and control latch circuits. Any one of the 128 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the D input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the cross-point array to be cascaded for matrix expansion.

Ordering Information

PMT8816AE-1	40 Pin PDIP	Tubes
PMT8816AP-1	44 Pin PLCC	Tubes

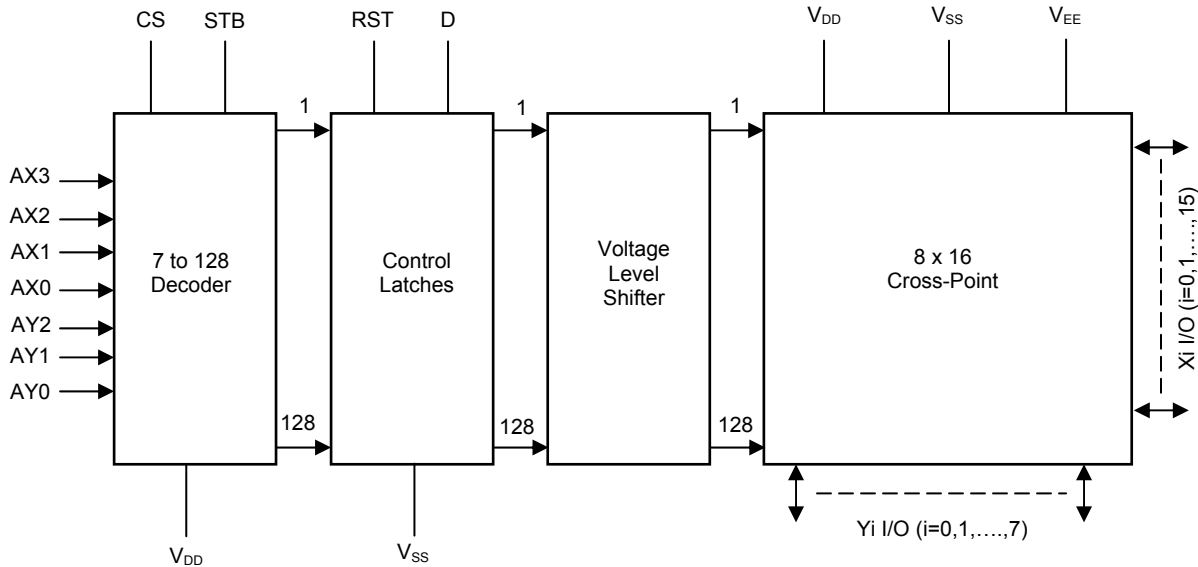


Figure 1: Functional Block Diagram

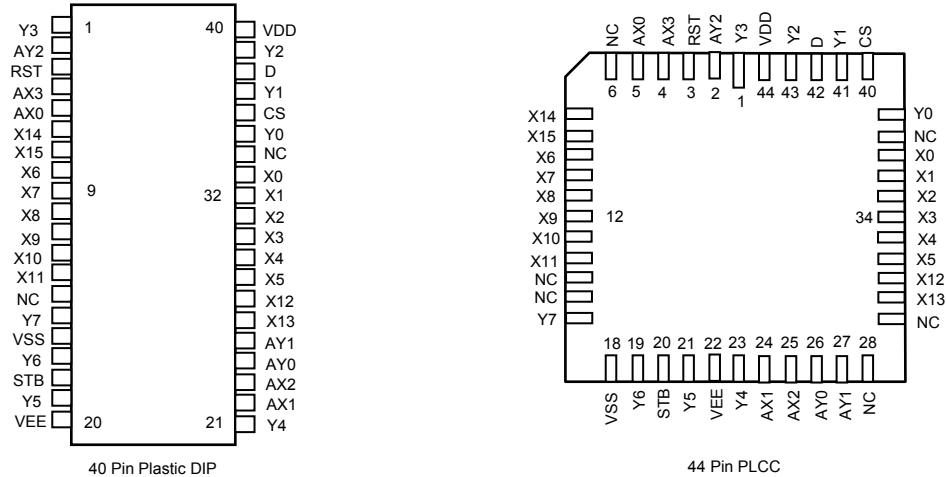


Figure 2: Pin Connections

Pin Description

Pin #		Name	Description
PDIP	PLCC		
1	1	Y3	Y3 Analog (Input/Output): this is connected to the Y3 column of the switch array.
2	2	AY2	Y2 Address Line (Input).
3	3	RST	Master RST (Input): this is used to turn off all switches regardless of the condition of CS. Active High.
4,5	4,5	AX3,AX0	X3 and X0 Address Lines (Inputs).
6,7	7,8	X14,X15	X14 and X15 Analog (Inputs/Outputs): these are connected to the X14 and X15 rows of the switch array.
8-13	9-14	X6-X11	X6-X11 Analog (Inputs/Outputs): these are connected to the X6-X11 rows of the switch array.
14	6,15,16	NC	No Connection
15	17	Y7	Y7 Analog (Input/Output): this is connected to the Y7 column of the switch array.
16	18	V _{SS}	Digital Ground Reference.
17	19	Y6	Y6 Analog (Input/Output): this is connected to the Y6 column of the switch array.
18	20	STB	STB (Input): enables function selected by address and data. Address must be stable before STB goes high and D must be stable on the falling edge of the STB. Active High.

Pin #		Name	Description
PDIP	PLCC		
19	21	Y5	Y5 Analog (Input/Output): this is connected to the Y5 column of the switch array.
20	22	V _{EE}	Negative Power Supply.
21	23	Y4	Y4 Analog (Input/Output): this is connected to the Y4 column of the switch array.
22,23	24,25	AX1,AX2	X1 and X2 Address Lines (Inputs).
24,25	26,27	AY0,AY1	Y0 and Y1 Address Lines (Inputs).
26,27	30,31	X13,X12	X13 and X12 Analog (Inputs/Outputs): these are connected to the X13 and X12 rows of the switch array.
28-33	32-37	X5-X0	X5-X0 Analog (Inputs/Outputs): these are connected to the X5-X0 rows of the switch array.
34	28,29,38	NC	No Connection.
35	39	Y0	Y0 Analog (Input/Output): this is connected to the Y0 column of the switch array.
36	40	CS	Chip Select (Input): this is used to select the device. Active High.
37	41	Y1	Y1 Analog (Input/Output): this is connected to the Y1 column of the switch array.
38	42	D	D (Input): a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	43	Y2	Y2 Analog (Input/Output): this is connected to the Y2 column of the switch array.
40	44	V _{DD}	Positive Power Supply.

Functional Description

The PMT8816 is an analog switch matrix of an 8 X 16 array. The switches are arranged as 8 columns and 16 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs.

The cross-point analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off.

The control unit consists of a 128 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the D input.

Data is asynchronously written into memory whenever both the CS (Chip Select) and STB inputs are high and are latched on the falling edge of STB.

A logic high written into a memory cell turns the corresponding cross-point switch ON and a logic low turns the cross-point OFF.

Only the cross-point switches corresponding to the addressed memory location are altered when data is written into memory.

The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected selecting the appropriate address bits.

A logic high on the RST input will asynchronously reset all memory locations to logic low turning off all cross-point switches regardless of whether CS is high or low.

Two voltage reference pins (V_{SS} and V_{EE}) are provided for the PMT8816 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE} .

The V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STB and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches.

The D input is buffered and is used as the input to all latches.

To enable a location, RST must be low and CS must go high while the address and data are set up. Then the STB input is set high and then low causing the data to be latched.

The data can be changed while STB is high, however, the corresponding switch will turn on and off in accordance with the D input. D must be stable on the falling edge of STB in order for correct data to be written to the latch.

Recommended Operating Conditions:

All voltages are with respect to V_{EE}

Characteristics	Sym.	Min	Typ.	Max.	Units
Operating Temperature	T_O	-40	25	85	°C
Supply Voltage	V_{DD} V_{SS}	4.5 V_{EE}		13.2 $V_{DD}-4.5$	V V
Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V
Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V

DC Electrical Characteristics:

Voltages are with respect to $V_{EE}=V_{SS}=0$ V, $V_{DD}=12$ V unless otherwise mentioned

Characteristics	Sym.	Min.	Max.	Units	Test Conditions
Quiescent Current Supply	I_{DD}		100	μ A	All digital inputs at V_{SS} or V_{DD}
			1.5	mA	All digital inputs at $2.4+V_{SS}; V_{SS}=7$ V
			15	mA	All digital inputs at 3.4 V
Off-State Leakage	I_{OFF}		500	nA	$ V_{Xi}-V_{Yi} =V_{DD}-V_{EE}$
Input logic "0" level	V_{IL}		0.8+ V_{SS}	V	$V_{SS}=6.5$ V; $V_{EE}=0$ V
Input logic "1" level	V_{IH}	2.0+ V_{SS}		V	
Input leakage (digital pins)	I_{LEAK}		10	μ A	All digital inputs at V_{SS} or V_{DD}

Switch Resistance

Characteristics	Sym.	25 °C	70 °C	85 °C	Units	Test Conditions
		Max.	Max.	Max.		
ON Resistance	R_{ON}	185	215	225	Ω	$V_{EE}=V_{SS}=0$ V, $V_{DD}=5$ V, $V_{Xi}=V_{DD}/2$ $ V_{Xi}-V_{Yi} =0.4$ V
		75	85	90		$V_{EE}=V_{SS}=0$ V, $V_{DD}=10$ V, $V_{Xi}=V_{DD}/2$ $ V_{Xi}-V_{Yi} =0.4$ V
		65	75	80		$V_{EE}=V_{SS}=0$ V, $V_{DD}=12$ V, $V_{Xi}=V_{DD}/2$ $ V_{Xi}-V_{Yi} =0.4$ V

AC Electrical Characteristics – Cross-point Performance:

Voltages are with respect to $V_{DD}=5\text{ V}$, $V_{SS}=0\text{ V}$, $V_{EE}=-7\text{ V}$, unless otherwise stated.

Characteristics	Sym.	Min.	Max	Units	Test Conditions
Switch I/O Capacitance	C_S		20	pF	$f=1\text{MHz}$
Feedthrough Capacitance	C_F		0.2	pF	$f=1\text{MHz}$
ON Frequency response	F_{3dB}	45		MHz	Switch ON; $V_{INA}=2V_{PP}$ sinewave; $R_L=1\text{ k}\Omega$
Total Harmonic Distortion	THD		0.04	%	Switch ON; $V_{INA}=2V_{PP}$ sinewave; $R_L=1\text{ k}\Omega$
OFF Channel feedthrough	FDT	-95		dB	Switch OFF; $V_{INA}=2V_{PP}$ sinewave; $f=1\text{ kHz}$; $R_L=1\text{ k}\Omega$
Cross-talk between any two channels	X_{TALK}			dB	$V_{INA}=2V_{PP}$ sinewave; $f=10\text{ MHz}$; $R_L=75\text{ }\Omega$
					$V_{INA}=2V_{PP}$ sinewave; $f=10\text{ kHz}$; $R_L=600\text{ }\Omega$
					$V_{INA}=2V_{PP}$ sinewave; $f=10\text{ kHz}$; $R_L=1\text{ k}\Omega$
					$V_{INA}=2V_{PP}$ sinewave; $f=1\text{ kHz}$; $R_L=10\text{ k}\Omega$
Propagation delay through switch	t_{PS}		30	ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$

AC Electrical Characteristics – Timing:

Voltages are with respect to $V_{DD}=5\text{ V}$, $V_{SS}=0\text{ V}$, $V_{EE}=-7\text{ V}$, unless otherwise stated.

Characteristics	Sym.	Min	Max	Units	Test Conditions
Control Input cross-talk to switch	CX_{talk}		30	mV _{PP}	$V_{IN}=3V_{PP}$ square wave; $R_{IN}=1\text{ k}\Omega$; $R_L=10\text{ k}\Omega$
Digital Input capacitance	CD_I		10	pF	$f=1\text{ MHz}$
Switching Frequency	F_O		20	MHz	
Setup time D to STB	t_{DS}	10		ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
Hold time D to STB	t_{DH}	10		ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
Setup time Address to STB	t_{AS}	10		ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
Hold time Address to STB	t_{AH}	10		ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
Setup time CS to STB	t_{DS}	10		ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
Hold time CS to STB	t_{DS}	10		ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
STB pulse width	t_{DS}	20		ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
RST pulse width	t_{DS}		40	ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
STB to switch status delay	t_{DS}		100	ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
D to switch status delay	t_{DS}		100	ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$
RST to switch status delay	t_{DS}		100	ns	$R_L=1\text{ k}\Omega$; $C_L=50\text{ pF}$

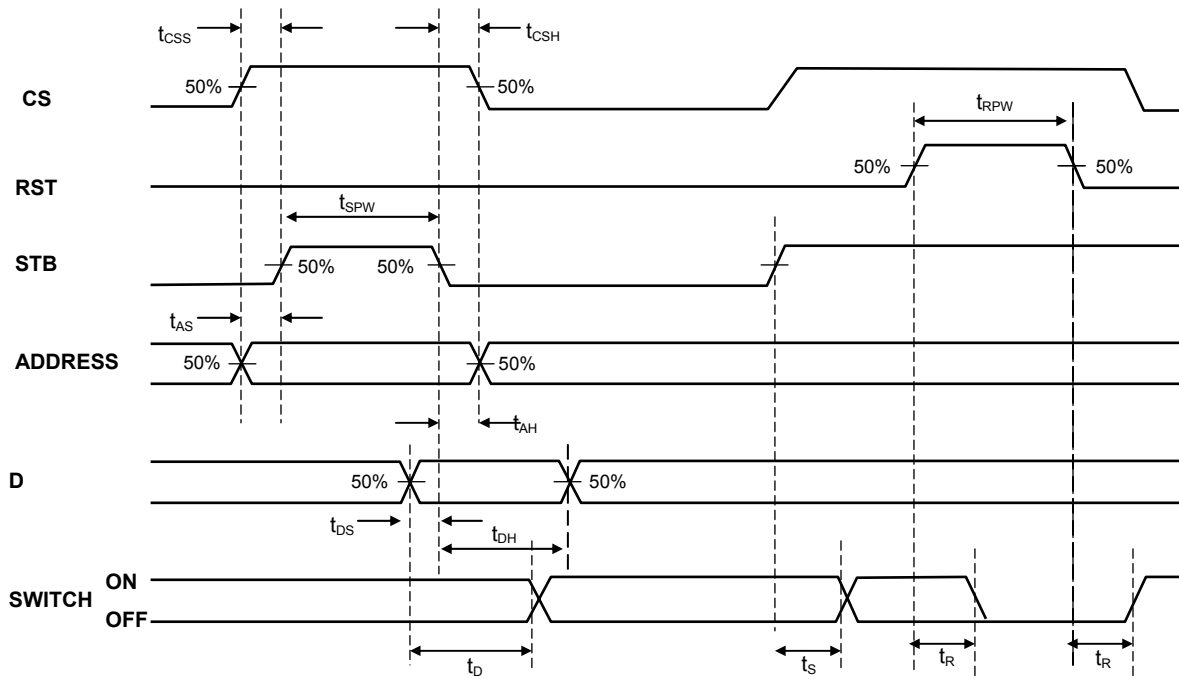
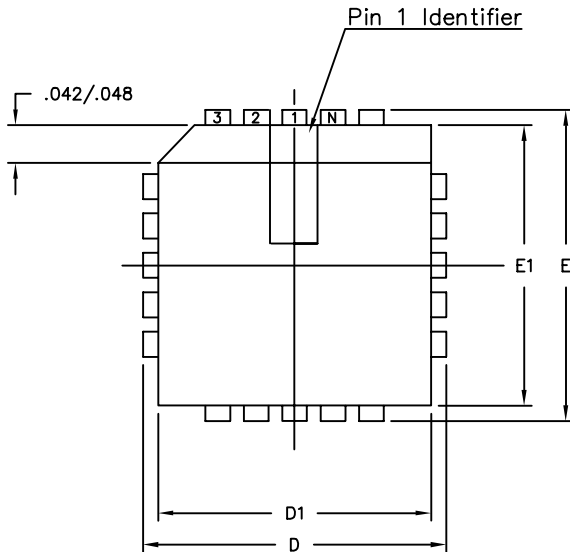


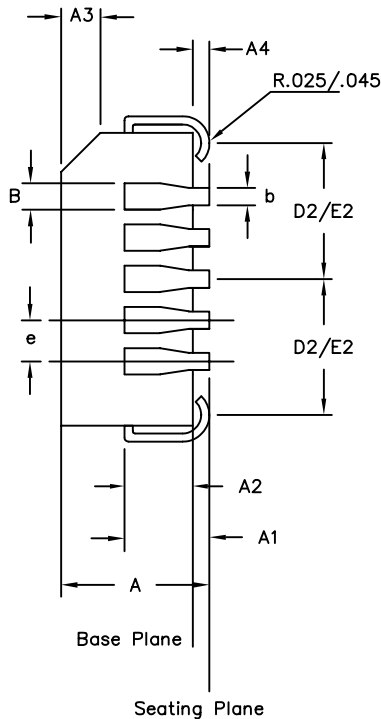
Figure 3: Timing Diagram

AX3	AX2	AX1	AX0	AY2	AY1	AY0	Connection
0	0	0	0	0	0	0	X0-Y0
0	0	0	1	0	0	0	X1-Y0
0	0	1	0	0	0	0	X2-Y0
0	0	1	1	0	0	0	X3-Y0
0	1	0	0	0	0	0	X4-Y0
0	1	0	1	0	0	0	X5-Y0
0	1	1	0	0	0	0	X12-Y0
0	1	1	1	0	0	0	X13-Y0
1	0	0	0	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
1	0	1	0	0	0	0	X8-Y0
1	0	1	1	0	0	0	X9-Y0
1	1	0	0	0	0	0	X10-Y0
1	1	0	1	0	0	0	X11-Y0
1	1	1	0	0	0	0	X14-Y0
1	1	1	1	0	0	0	X15-Y0
0	0	0	0	0	0	1	X0-Y1
.
1	1	1	1	1	1	1	X15-Y1
0	0	0	0	0	0	0	X0-Y2
.
1	1	1	1	1	1	1	X15-Y2
0	0	0	0	0	0	1	X0-Y3
.
1	1	1	1	1	1	1	X15-Y3
0	0	0	0	0	1	0	X0-Y4
.
1	1	1	1	1	1	1	X15-Y4
0	0	0	0	0	1	0	X0-Y5
.
1	1	1	1	1	1	1	X15-Y5
0	0	0	0	0	1	1	X0-Y6
.
1	1	1	1	1	1	1	X15-Y6
0	0	0	0	0	1	1	X0-Y7
.
1	1	1	1	1	1	1	X15-Y7

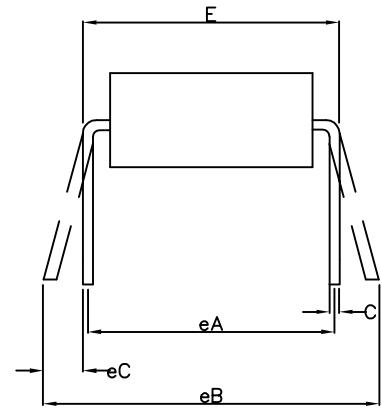
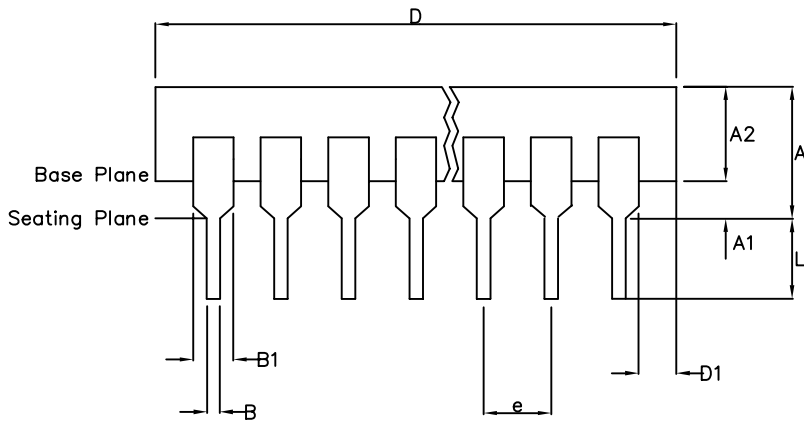
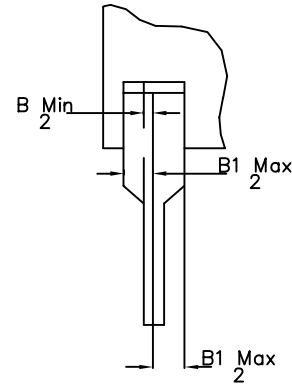
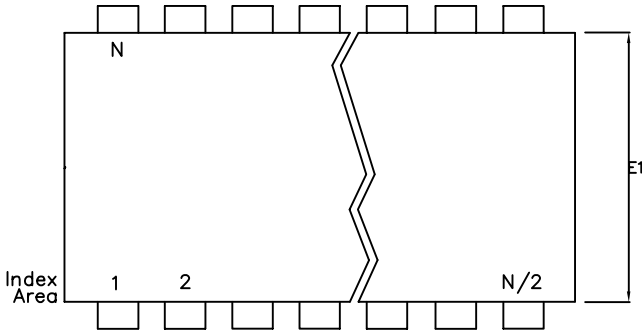
Table I: Truth table

Package outline and Dimensions
44 Lead PLCC


Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	—	0.51	—
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050	BSC	1.27	BSC
Pin features				
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				



Package Outline and Dimensions
40pin PDIP



	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	40		40	
Conforms to Jeduc MS-011AC ISS.B				