

Features

- 2.7V to 5.5V operation
- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode

Applications

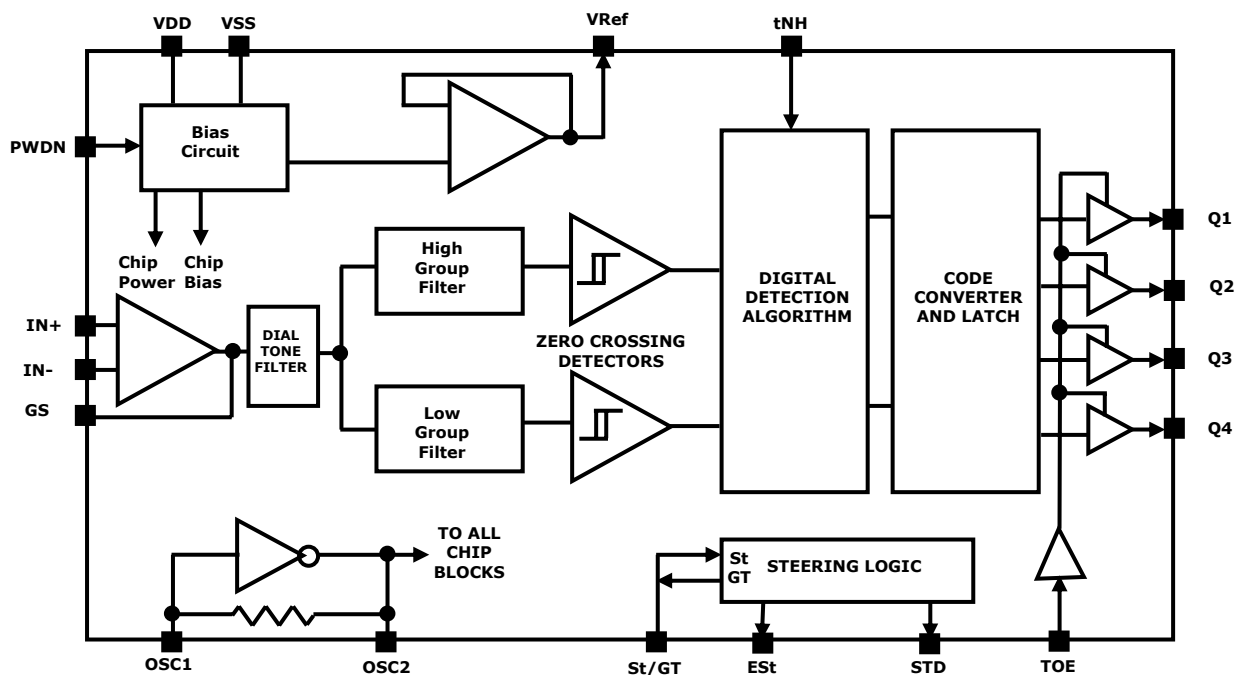
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Description

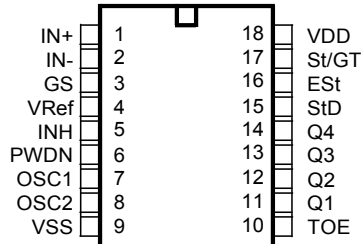
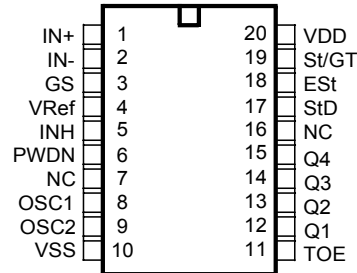
The PMT9370 is a complete DTMF receiver integrating both the band-split filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

Ordering Information

PMT9370AE1	18 Pin PDIP	Tubes
PMT9370AN1	20 Pin SSOP	Tubes
PMT9370AS1	18 Pin SSOP	Tubes
PMT9370ANR1	20 pin SSOP	Tape and Reel



Functional Block Diagram


18 PIN PLASTIC DIP/SOIC

20 PIN SSOP
Figure 2 - Pin Connections
Pin Descriptions

Pin #		Name	Description
18	20		
1	1	IN+	Non-Inverting Op-Amp (Input).
2	2	IN-	Inverting Op-Amp (Input).
3	3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V _{Ref}	Reference Voltage (Output). Nominally V _{DD} /2 is used to bias inputs at mid-rail (see Figure 5 and Figure 6).
5	5	INH	Inhibit (Input). Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	Power Down (Input). Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	Clock (Input).
8	9	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	VSS	Ground (Input). 0 V typical.
10	11	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	17	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V _{TSt} .
16	18	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.

Pin #		Name	Description
18	20		
17	19	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	20	VDD	Positive power supply (Input). +3 V typical.
	7, 16	NC	No Connection.

Functional Description

The PMT9370 monolithic DTMF receiver offers small size, low power consumption and high performance, with 3 volt operation. Its architecture consists of a band-split filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band-pass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section which smoothes the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_C (see Figure 3) to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives v_C to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Digit	TOE	INH	Est	Q ₄	Q ₃	Q ₂	Q ₁
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1 - Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
 X = DON'T CARE

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 3 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see Figure 7) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μ F is recommended for most applications, leaving R to be selected by the designer.

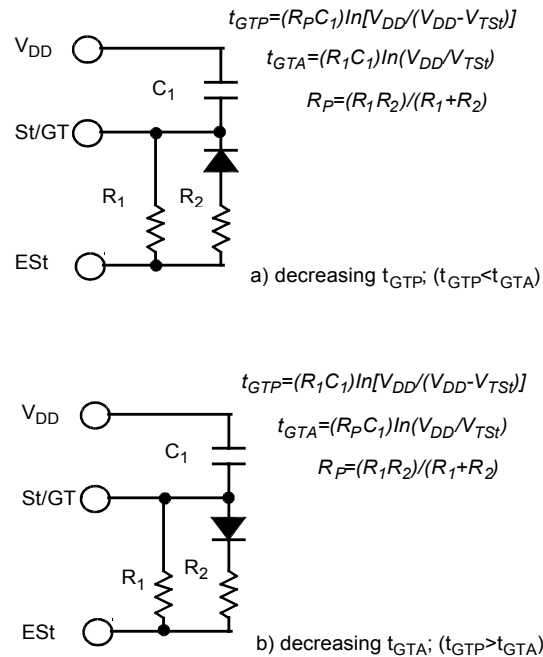


Figure 3 - Guard Time Adjustment

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and inter-digital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

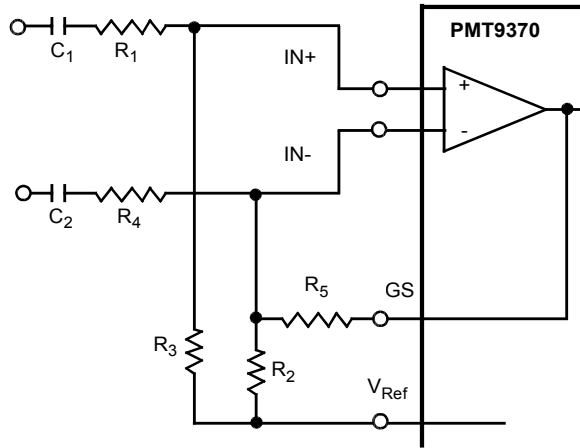
Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

Differential Input Configuration

The input arrangement of the PMT9370D/PMT9370D-1 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and V_{Ref} biasing the input at $1/2 V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5 .

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 6 (Single-Ended Input Configuration). However, it is possible to configure several PMT9370 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 5 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.



Differential Input Amplifier

$C_1=C_2=10\text{ nF}$
 $R_1=R_4=R_5=100\text{ k}\Omega$ All resistors are $\pm 1\%$ tolerance.
 $R_2=60\text{ k}\Omega, R_3=37.5\text{ k}\Omega$ All capacitors are $\pm 5\%$ tolerance.

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

$$\text{VOLTAGE GAIN } (A_v \text{ diff}) = \frac{R_5}{R_1}$$

INPUT IMPEDANCE

$$(Z_{\text{INDIFF}}) = 2 \sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 4 - Differential Input Configuration

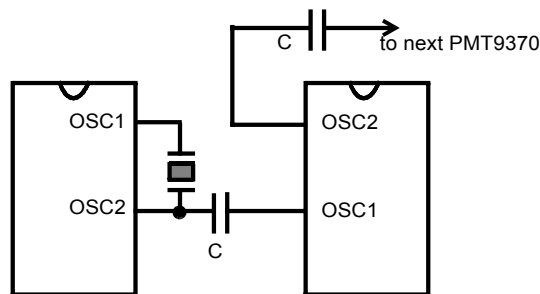


Figure 5 - Oscillator Connection

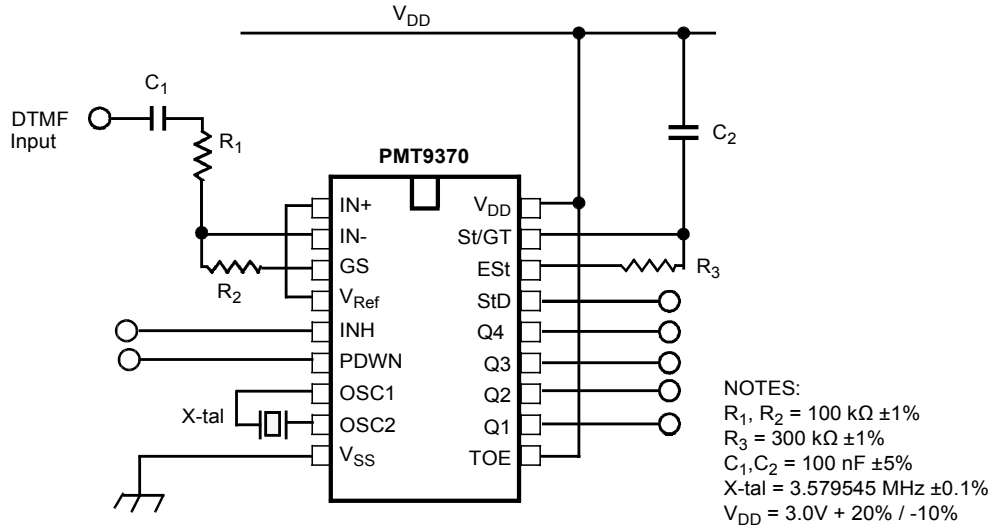


Figure 6 - Single-Ended Input Configuration

Absolute Maximum Ratings

	Parameter	Symbol	Min.	Max.	Units
1	DC Power Supply Voltage	V_D		7	V
2	Voltage on any pin	V_I	$V_{SS}-0.3$	$V_{DD}+0.3$	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{ST}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

Recommended operating conditions

	Parameter	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	2.5	3	5.5	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	Crystal/Clock Frequency	f_c		3.579545		MHz	
4	Crystal/Clock Freq. Tolerance	Δf_c		±0.1		%	

DC Electrical Characteristics

		Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		1	10	μA	PWDN= V_{DD}
2		Operating supply current	I_{DD}		3.0	6.5	mA	
3		Power consumption	P_O		15		mW	$f_c=3.579545$ MHz
4	INPUTS	High level input	V_{IH}	3.5			V	$V_{DD} = 3.0$ V
5		Low level input voltage	V_{IL}			1.5	V	$V_{DD} = 3.0$ V
6		Input leakage current	I_{IH}/I_{IL}		0.05	5	μA	$V_{IN} = V_{SS}$ or V_{DD}
7		Pull up (source) current	I_{SO}		7	15	μA	TOE (pin 10) = 0, $V_{DD} = 3.0$ V
8		Pull down (sink) current	I_{SI}		15	40	μA	INH = V_{DD} , PWDN = V_{DD} , $V_{DD} = 3.0$ V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}		0.465 V_{DD}		V	
11	OUTPUTS	Low level output voltage	V_{OL}			0.03	V	No load
12		High level output voltage	V_{OH}	$V_{DD}-0.03$			V	No load
13		Output low (sink) current	I_{OL}	1.5	8		mA	$V_{OUT} = 0.4$ V
14		Output high (source) current	I_{OH}	1.0	3.0		mA	$V_{OUT} = 3.6$ V, $V_{DD} = 3.6$ V
15		V_{Ref} output voltage	V_{Ref}	2.4		2.7	V	No load
16		V_{Ref} output resistance	R_{OR}		10		kΩ	

Operating Characteristics
Gain Setting Amplifier

	Characteristics	Sym.	Min.	Typ. [‡]	Max.	Units	Test Conditions
1	Input leakage current	I _{IN}			100	nA	V _{SS} ≤ V _{IN} ≤ V _{DD}
2	Input resistance	R _{IN}	10			MΩ	
3	Input offset voltage	V _{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40	60		dB	V _{SS} + 0.75 V ≤ V _{IN} ≤ V _{DD} -0.75 biased at V _{Ref} = 1.5 V
6	DC open loop voltage gain	A _{VOL}	32	65		dB	
7	Unity gain bandwidth	f _C	0.30	1.5		MHz	
8	Output voltage swing	V _O		2.2		V _{pp}	Load ≥ 100 kΩ to V _{SS} @ GS
9	Maximum capacitive load (GS)	C _L			100	pF	
10	Resistive load (GS)	R _L			50	kΩ	
11	Common mode range	V _{CM}		1.5		V _{pp}	No Load

AC Electrical Characteristics

	Characteristics	Sym	Min.	Typ [‡]	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-34		-4.0	dBm	1,2,3,5,6,9 Min @ V _{DD} =3.6 V Max @ V _{DD} =2.7 V
			15.4		489	mV _{RMS}	
2	Negative twist accept				9	dB	2,3,6,9,12
3	Positive twist accept				9	dB	2,3,6,9,12
4	Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
5	Frequency deviation reject		±3.5%				2,3,5,9
6	Third zone tolerance			-16		dB	2,3,4,5,9,10
7	Noise tolerance			-12		dB	2,3,4,5,7,9,10
8	Dial zone tolerance			+22		dB	2,3,4,5,8,9,11

*** NOTES**

1. dBm =decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have equal amplitude.
6. Tone pair is deviated by ±1.5%± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

AC Electrical Characteristics

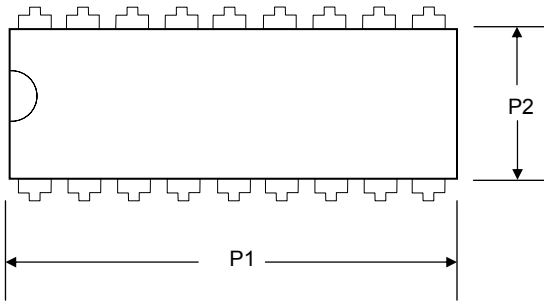
		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	TIMING	Tone present detect time	t _{DP}	5	11	14	ms	Note 1
2		Tone absent detect time	t _{DA}	0.5	4	8.5	ms	Note 1
3		Tone duration accept	t _{REC}			40	ms	Note 2
4		Tone duration reject	t _{REC}	20			ms	Note 2
5		Interdigit pause accept	t _I			40	ms	Note 2
6		Interdigit pause reject	t _{DO}	20			ms	Note 2
7	OUTPUTS	Propagation delay (St to Q)	t _{PQ}			11	µs	TOE=V _{DD}
8		Propagation delay (St to StD)	t _{PStD}			20	µs	TOE=V _{DD}
9		Output data set up (Q to StD)	t _{QStD}		5.0		µs	TOE=V _{DD}
10		Propagation delay (TOE to Q ENABLE)	t _{PTE}		50		ns	load of 10 kΩ, 50 pF
11		Propagation delay (TOE to Q DISABLE)	t _{PTD}		130		ns	load of 10 kΩ, 50 pF
12	PDWN	Power-up time	t _{PJ}		30		ms	Note 3
13		Power-down time	t _{PD}		20		ms	
14	CLOCK	Crystal/clock frequency	f _C	3.5759	3.5795	3.5831	MHz	
15		Clock input rise time	t _{LHCL}			110	ns	Ext. clock
16		Clock input fall time	t _{HLCL}			110	ns	Ext. clock
17		Clock input duty cycle	DC _{CL}	40	50	60	%	Ext. clock
18		Capacitive load (OSC2)	C _{LO}			30	pF	

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

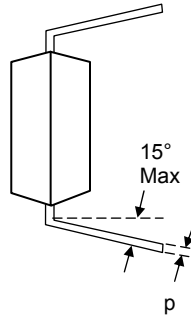
***NOTES:**

1. Used for guard-time calculation purposes only and tested at -4 dBm.
2. These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
3. With valid tone present at input, t_{PJ} equals time from PDWN going low until Est going high.

Package Layout and Dimensions

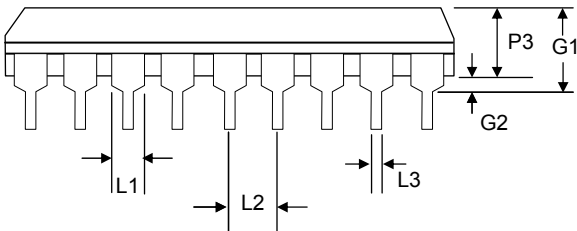


Top View

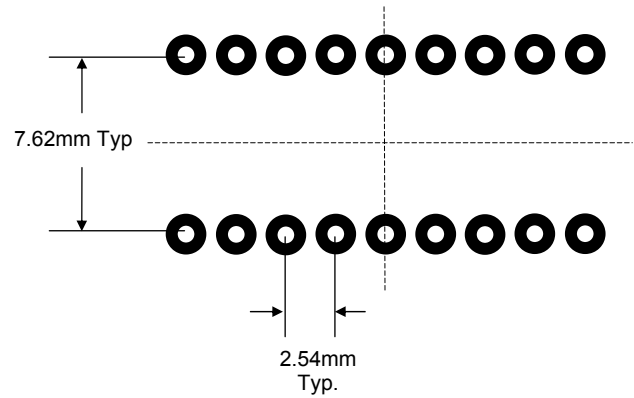


End View

Dim	MILLIMETERS	
	MIN	MAX
P1	23.09	23.14
P2	6.25	6.65
P3	3.3	3.7
L1	1.52	1.58
L2	2.54	2.54
L3	0.40	0.48
p	0.20	0.30
G1	4.36	4.36
G2	3.0Min	

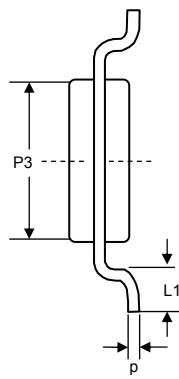
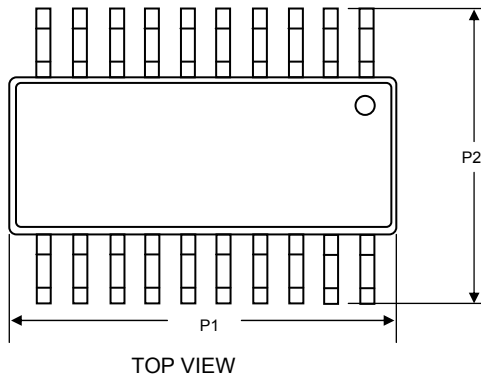


Side View

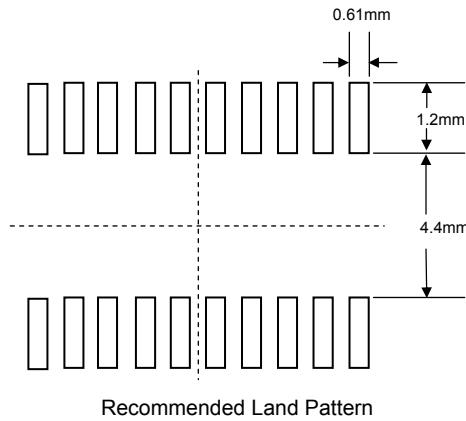
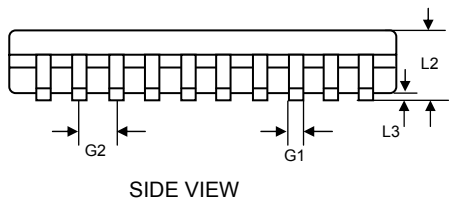


Recommended Pattern Layout

Package Outline and Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
P1	11.35	11.75	0.447	0.462
P2	10.00	10.65	0.394	0.419
P3	7.40	7.50	0.291	0.299
L1	0.4	1.27	0.016	0.050
L2	2.35	2.65	0.093	0.104
L3	0.10	0.30	0.004	0.012
p	0.23	0.32	0.009	0.013
G1	0.33	0.51	0.013	0.020
G2	1.27 BSC		0.050 BSC	



Tape and Reel Specifications (Dimensions in mm)

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P1	t _{max}
178 (7")	10.80±0.10	12.30±0.10	0.80±0.10	1.50±0.10	1.75±0.10	7.50±0.05	16.00±0.30	4.00±0.10	2.00±0.05	12.00±0.10	0.25

