

Features

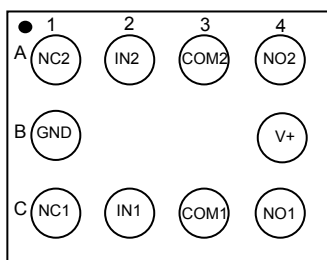
- Low Voltage Operation
- Low On-Resistance $R_{on} = 0.25\Omega @ 2.7 V$
- $-69 \text{ dB } O_{IRR} @ 2.7 V, 100 \text{ kHz MSOP-10}$ and DFN-10 Packages ESD Protection $>2000 V$
- Latch-Up Current $>300 \text{ mA}$ (JESD 78)

Benefits

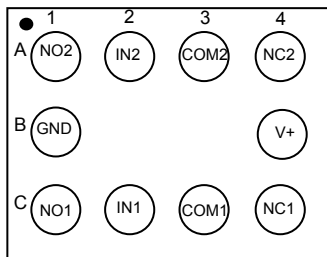
- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.8-V Logic Compatible
- High Bandwidth

Applications

- Cellular Phones
- Speaker Headset Switching Audio
- Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement
- USB1.1

PA3535


Top View

PA3536


Top View

Truth Table

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

Description

The PA3535/PA3536 are 0.25Ω dual SPDT analog switches designed for low voltage applications.

The PA3535/PA3536 has on-resistance matching (less than $0.05\Omega @ 2.7 V$) and flatness (less than $0.2\Omega @ 2.7 V$) that is guaranteed, over the entire voltage range. Additionally, low logic thresholds make the PA3535/PA3536 an ideal interface to low voltage DSP control signals.

The PA3535/PA3536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is $-69 \text{ dB} @ 100 \text{ kHz}$.

The PA3535/PA3536 contains the additional benefit of 2,000 Volt ESD protections.

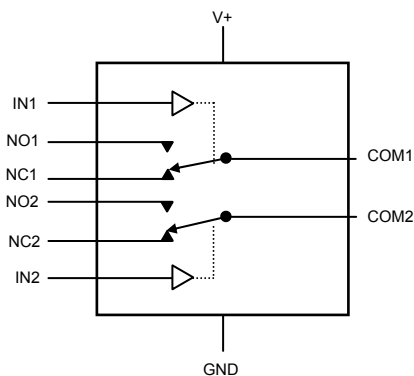
In space saving CSP (Pb-free) packages, the PA3535/PA3536 are high performance, low R_{on} switches for battery powered applications.

No (Pb) is used in the manufacturing process either inside the device/package or on the external terminations.

As a committed partner to the community and the environment, ProTek Analog manufactures this product with the lead (Pb)-free device terminations.

The different lead (Pb)-free materials are interchangeable and meet all JEDEC standards for reflow and MSL rating.

Functional Diagram



Ordering Information

Temp Range	Package	Part Number
-40 to +80°C	Flip Chip	PA3535-T7
	10 Bump	PA3536-T7

Absolute Maximum Ratings

Reference to Ground

V+.....-0.3 to +6.0V
IN, COM, NC, NO.....-0.3 to (V+ +0.3V)
Continuous Current (NO, NC, COM).....300mA

Peak Current.....500mA
(Pulsed at 1mS, 10% Duty Cycle)
Storage Temperature (D Suffix).....-65 to 150°C
ESD per Method 3015.7.....> 2KV
Power Dissipation.....457mWATT

NOTES

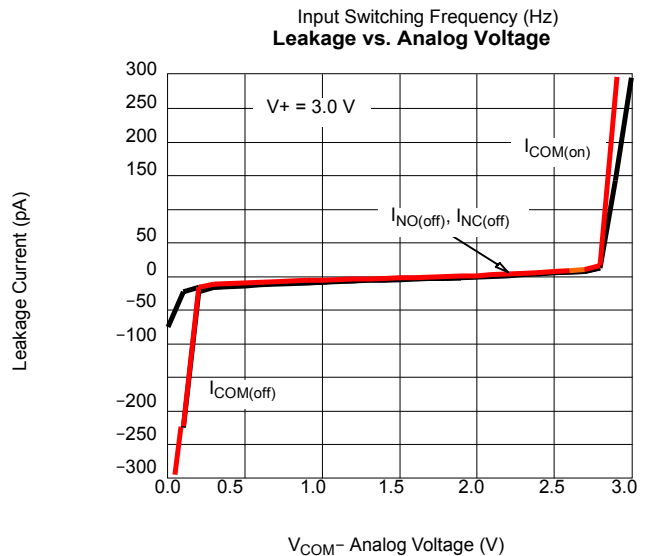
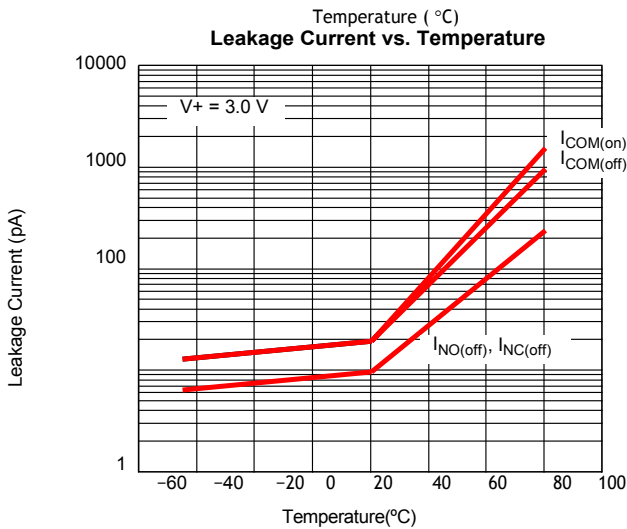
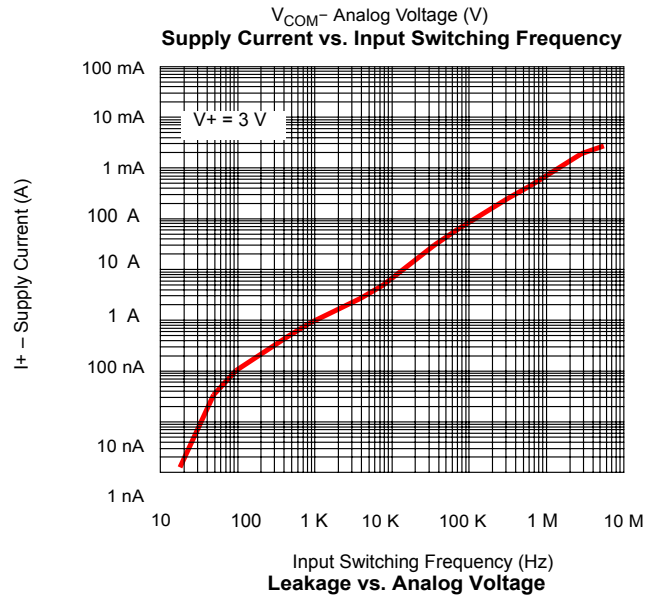
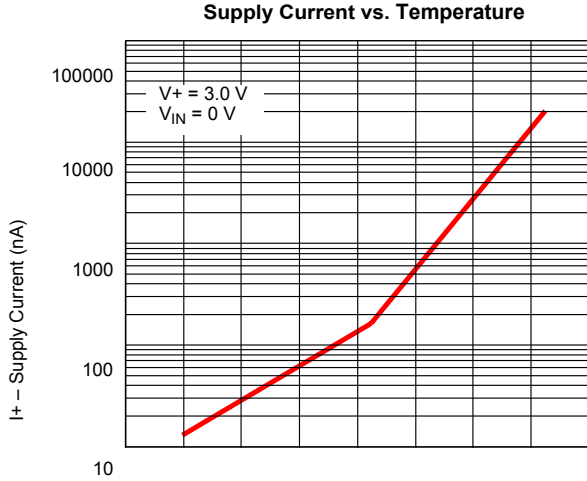
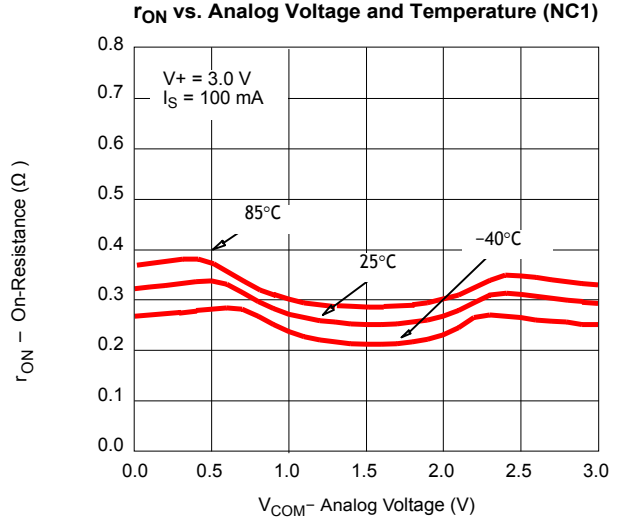
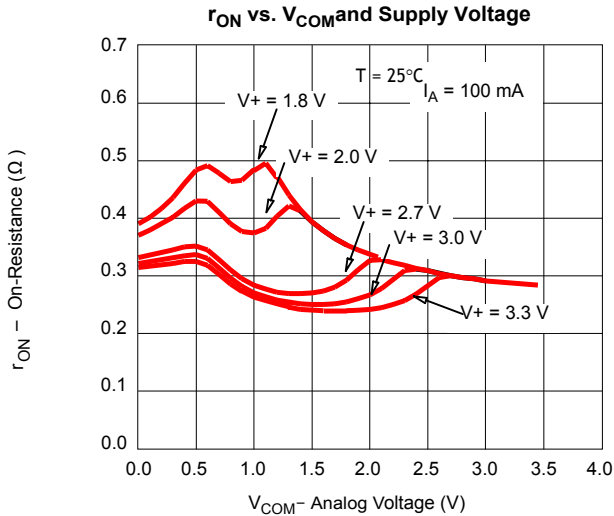
- a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered to PC Board.
- c. Derate 5.7 mW/ °C above 70 °C

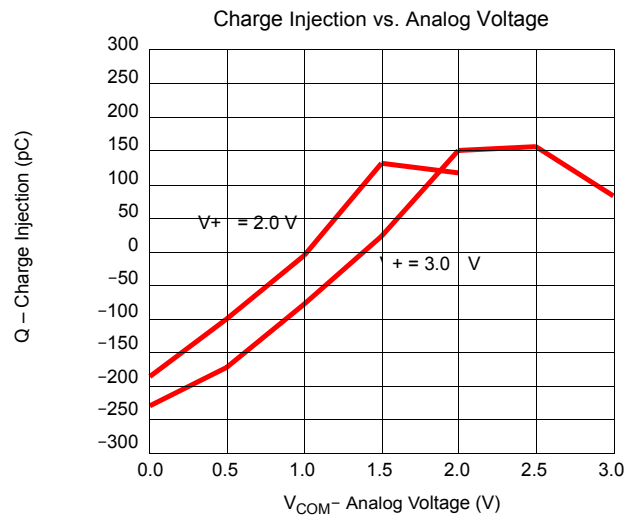
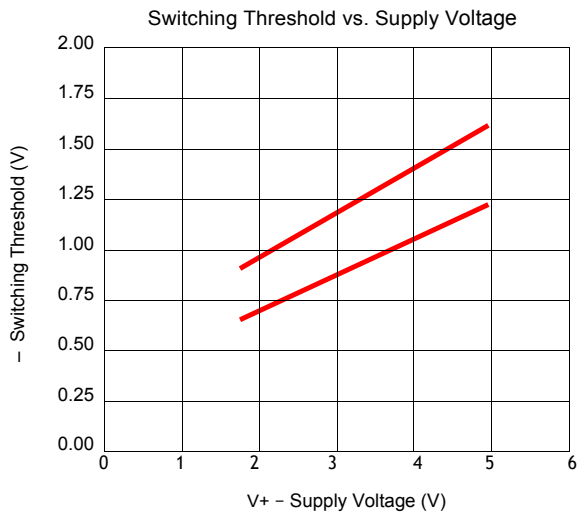
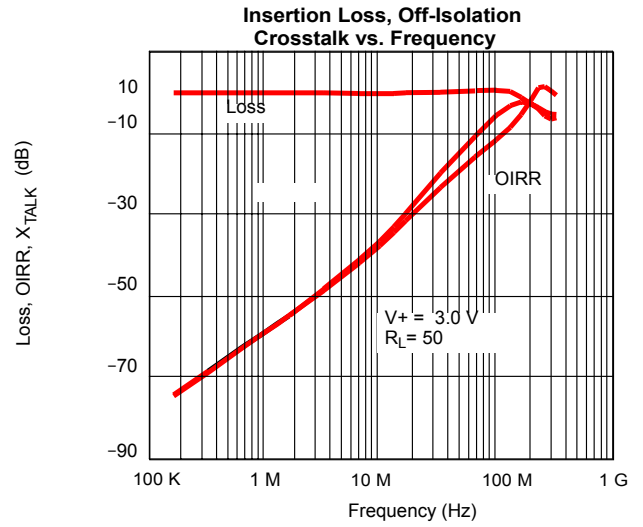
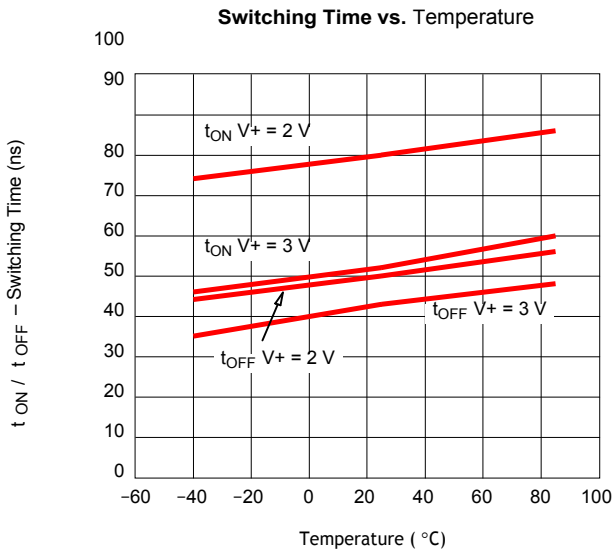
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Specification V+ = 3.0V Test Conditions unless otherwise specified: $V_+ = 3.0V \pm 10\%$, $V_{IN} = 0.4V$ or $2.0V$

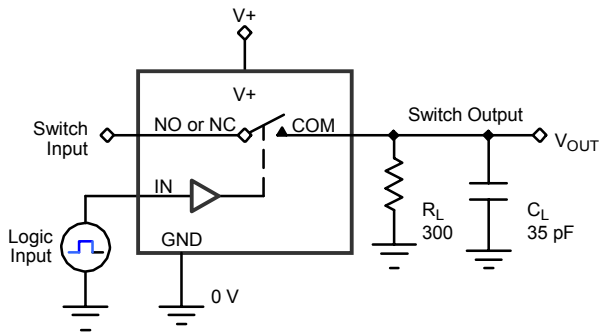
Parameter	Symbol	Test Conditions	Temp	Min	Typ	Max	Unit
Analog Switch							
Analog Signal Range	V_{NO}, V_{NC}, V_{COM}		Full	0.0		V_{CC}	V
On-Resistance	R_{ON}	$V_{CC} = 2.7V, V_{COM} = 0.9V - 1.5V$ $I_{NO}, I_{NC} = 50mA,$	Room		0.25	0.4	Ω
R_{ON} Matching	ΔR_{ON}		Full			0.05	
R_{ON} Flatness	$R_{ON(FLAT)}$				0.09	0.15	
Switch Off Leakage Current	$I_{OFF(NO)}$ or $I_{OFF(NC)}$	$V_+ = 3.3V,$ $V_{NO}, V_{NC} = 1.0V/3.0V, V_{COM} = 3.0V/1.0V$	Room	-1		-1	nA
	$I_{COM(OFF)}$		Full	-10		-10	
Channel On Leakage Current	$I_{COM(ON)}$	$V_+ = 3.3V, V_{NO}, V_{NC} = V_{COM} = 1.0V/3.0V$	Room	-1		-1	
Full			Full	-10		-10	
Digital Control							
Input High Voltage	V_{INH}		Full	2.0			V
Input Low Voltage	V_{INL}		Full			0.5	
Input Capacitance	C_{in}		Full		10		pF
Input Current	I_{INL} or I_{INH}	$V_{IN} = 0$ or V_+	Full	1		1	μA
Dynamic Characteristics							
Turn On Time	t_{ON}	V_{NO} or $V_{NC} = 2.0V, R_L = 300\Omega, C_L = 35pF$	Room		52	82	nS
Turn Off Time	t_{OFF}		Full		43	73	
Break Before Make Time	t_{BBM}		Full	1	6	78	
Charge Injection	Q_{INJ}	$C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0\Omega$	Room		21		pC
Off Isolation	OIRR	$R_L = 50\Omega, C_L = 5pF, f = 1MHz$	Room		-69		dB
Crosstalk	X_{TALK}		Room		-69		
NO, NC OFF Capacitance	$C_{NO(off)}$ $C_{NC(off)}$	$V_{IN} = 0$ or $V_+, f = 1MHz$	Room		145		pF
Channel On Capacitance	C_{ON}		Room		406		
Power Supply							
Supply Range	V_+	$V_{IN} = 0$ or V_+		1.8		5.5	V
Supply Current	I_+				0.01		1.0

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



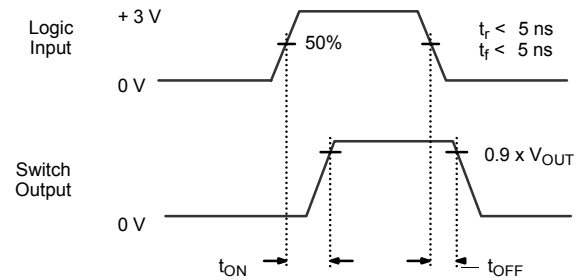


Test Circuits



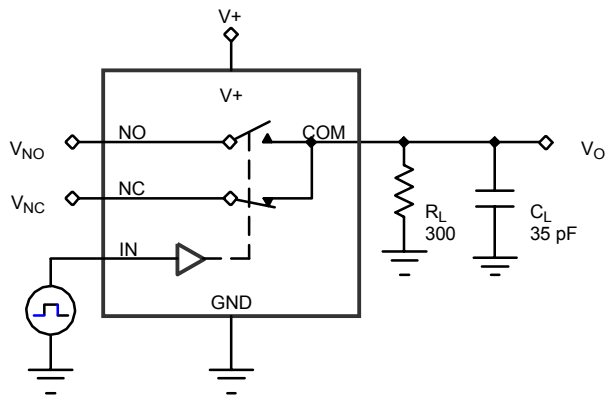
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



C_L (includes fixture and stray capacitance)

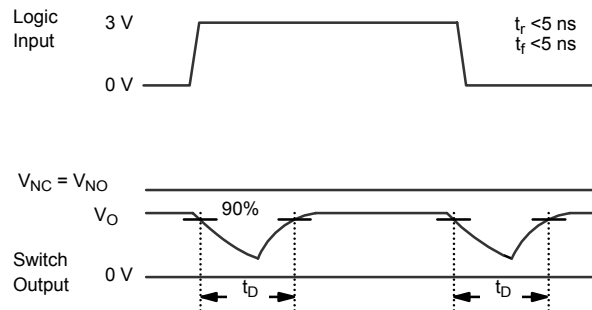
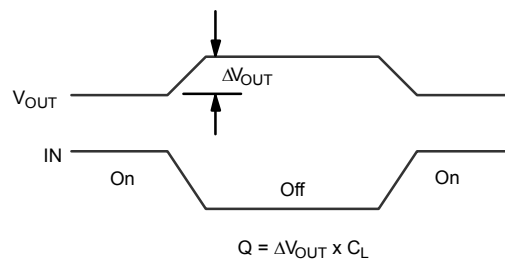
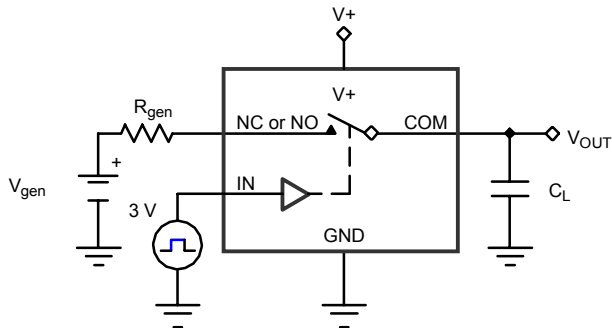


Figure 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

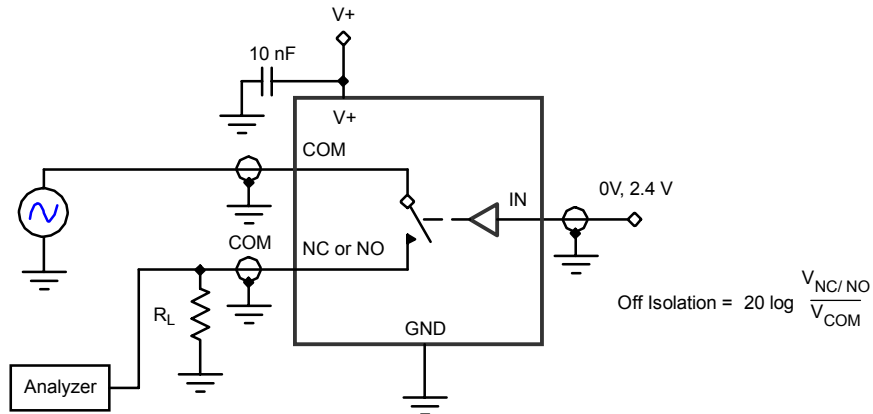


Figure 4. Off-Isolation

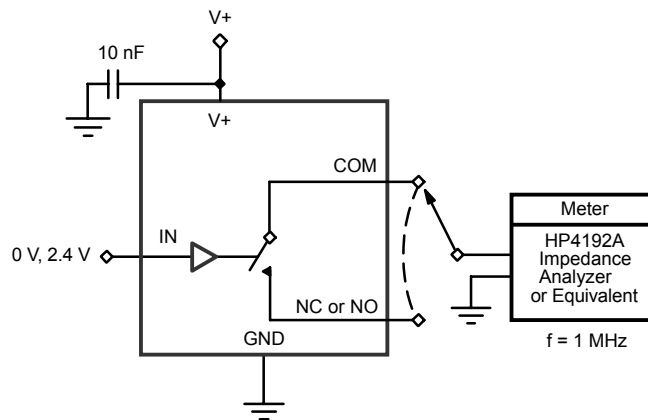
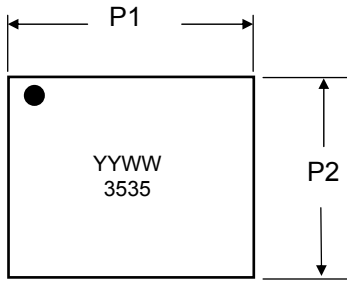
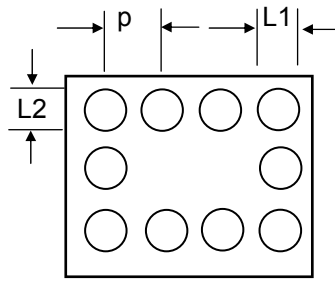


Figure 5. Channel Off/On Capacitance

Package Outline and Dimensions Flip-Chip 10-Bump

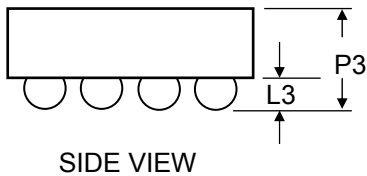


TOP VIEW

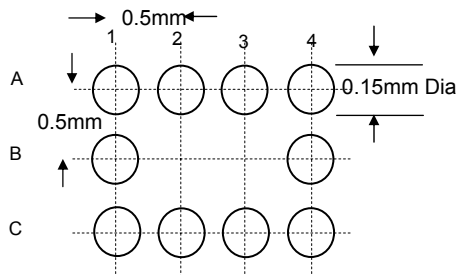


BOTTOM VIEW

Dim	MILLIMETERS		
	MIN	TYP	MAX
P1	1.98	2.00	2.02
P2	1.49	1.50	1.52
P3	0.68	0.71	0.75
L1	0.30	0.32	0.34
L2	0.30	0.32	0.34
L3	0.22	0.24	0.26
p	0.50	0.50	0.50



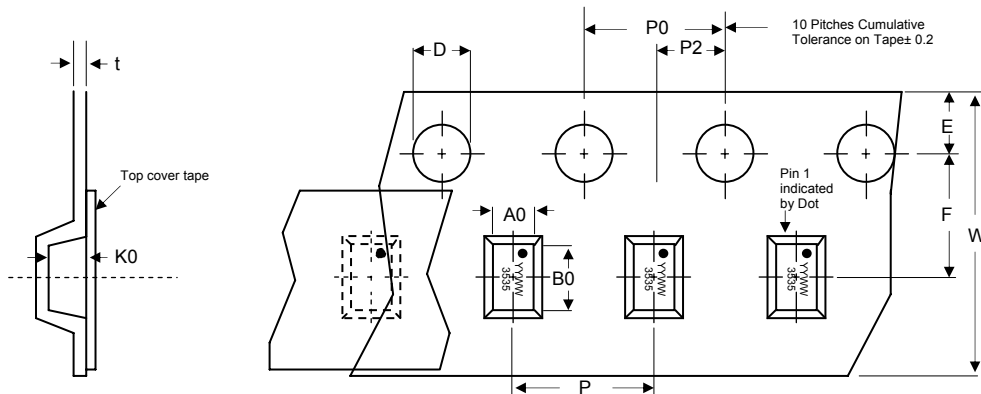
SIDE VIEW



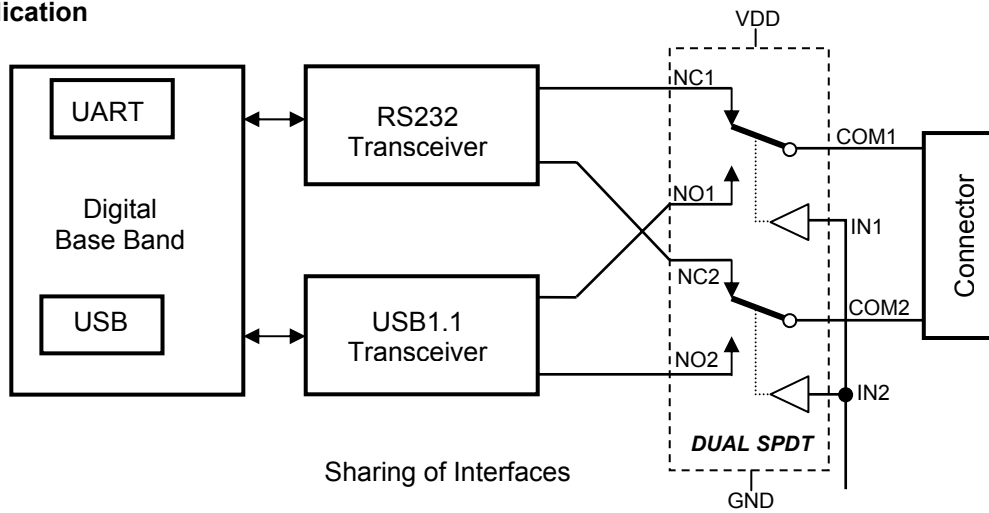
Recommended Land Pattern

Tape and Reel Specifications

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7")	1.68±0.10	2.18±0.10	0.85±0.10	1.50±0.10	1.75±0.10	3.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25



Typical application



Life Support Policy

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